

# Compal Confidential

## C560 LA-A061P Schematics Document

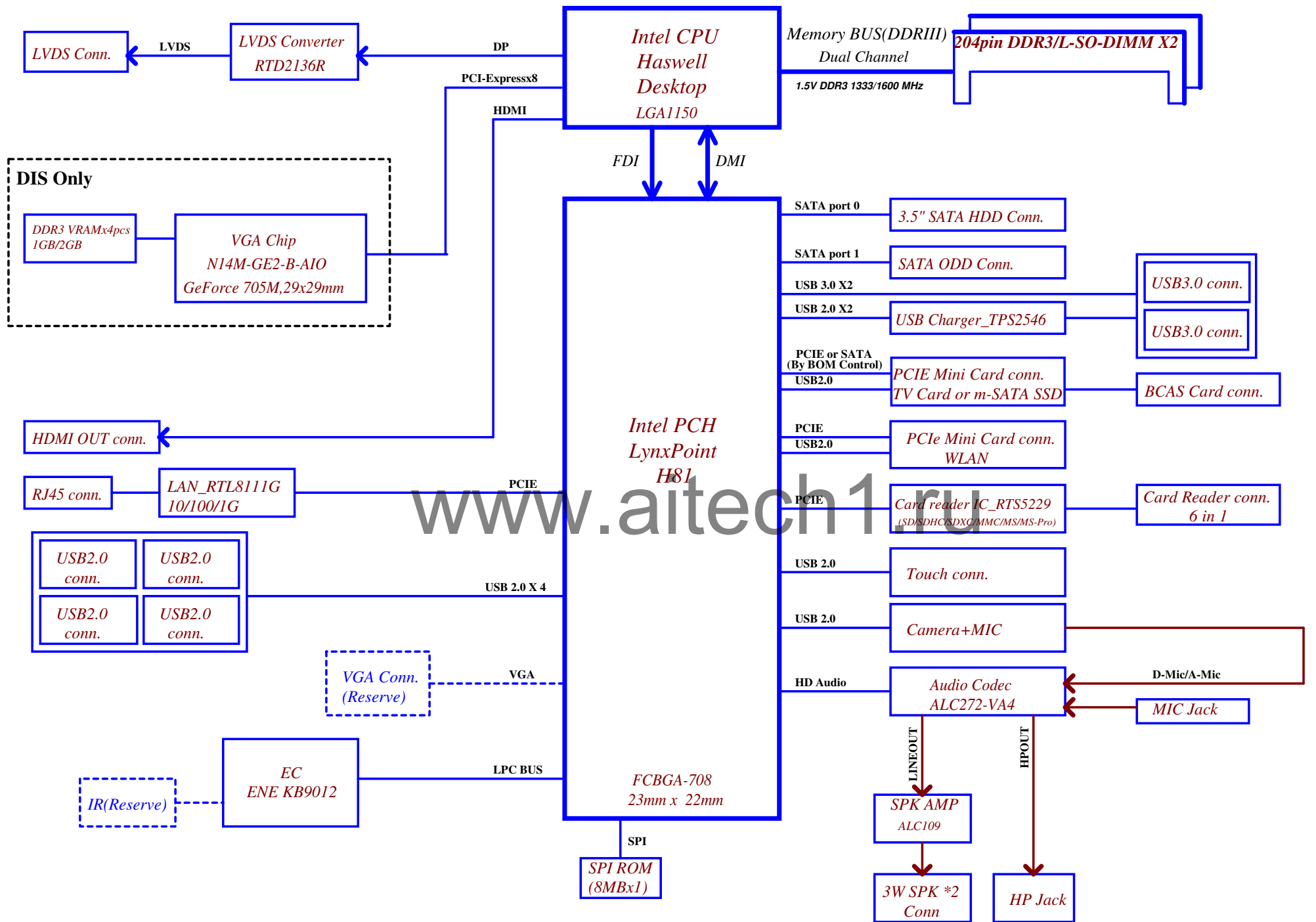
INTEL Haswell CPU with DDRIII + PCH Lynx-Point

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September 24, 2013

REV:1.0

|   |                    |                 |            |                          |                             |               |
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|   |                    |                 |            | Custom                   | ZEA00 LA-A061P M/B          | 0.3           |
|   |                    |                 |            | Date:                    | Tuesday, September 24, 2013 | Sheet 1 of 59 |

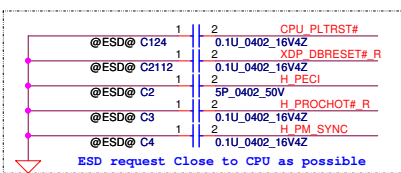


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| Issued Date  | 2013/04/01 | Deciphered Date    | 2014/04/01 | Title                    | Block Diagram               |       |   |    |    |
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|  |            |                    |            | Date:                    | Tuesday, September 24, 2013 | Sheet | 2 | of | 59 |
|  |            |                    |            |                          |                             |       |   |    |    |
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|  |            |                    |            |                          |                             |       |   |    |    |





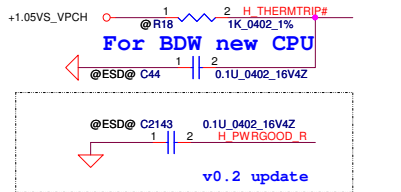
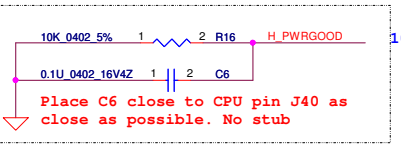




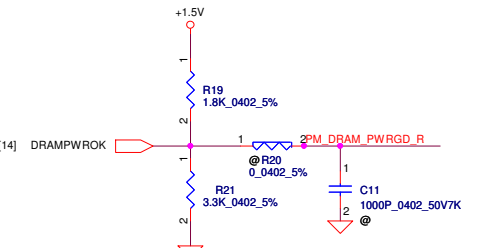
PECI 10mil spacing and Max Length < 15"

R11 follow CDB R42PR add 0ohm serial resistor

R12 follow CDB R34PR add 0ohm serial resistor



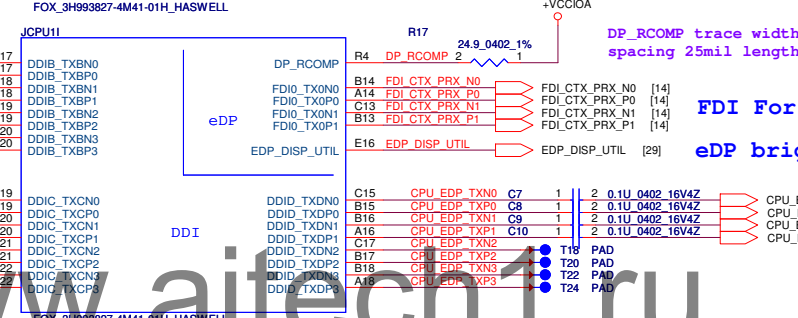
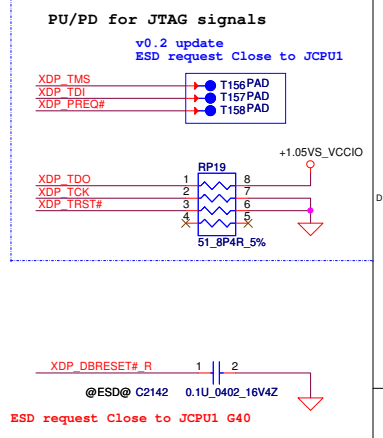
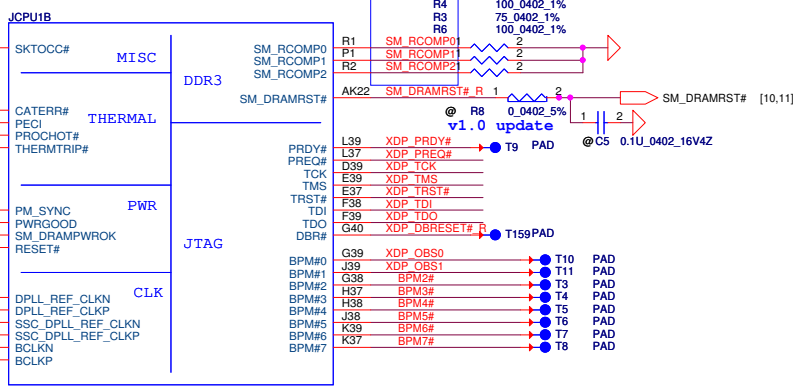
| Port   | Digital Display Interface (Differential Pairs) | HDMI Signals | Processor Digital Display Interface Pins |
|--------|--|--------------|--|
| Port B | DDIB_TXB0                                      | HDMIb_TX2_DP | DDIB_TXB(0)                              |
|        | DDIB_TXB1                                      | HDMIb_TX2_DN | DDIB_TXB(0)                              |
|        | DDIB_TXB2                                      | HDMIb_TX1_DP | DDIB_TXB(1)                              |
|        | DDIB_TXB3                                      | HDMIb_TX1_DN | DDIB_TXB(1)                              |
|        | DDIB_TXB4                                      | HDMIb_TX0_DP | DDIB_TXB(2)                              |
|        | DDIB_TXB5                                      | HDMIb_TX0_DN | DDIB_TXB(2)                              |
|        | DDIB_TXB6                                      | HDMIb_CLK_DP | DDIB_TXB(3)                              |
|        | DDIB_TXB7                                      | HDMIb_CLK_DN | DDIB_TXB(3)                              |
|        | DDIB_TXB8                                      | HDMIb_CLK_DP | DDIB_TXB(3)                              |
|        | DDIB_TXB9                                      | HDMIb_CLK_DN | DDIB_TXB(3)                              |
| Port C | DDIC_TXC0                                      | HDMIc_TX2_DP | DDIC_TXC(0)                              |
|        | DDIC_TXC1                                      | HDMIc_TX2_DN | DDIC_TXC(0)                              |
|        | DDIC_TXC2                                      | HDMIc_TX1_DP | DDIC_TXC(1)                              |
|        | DDIC_TXC3                                      | HDMIc_TX1_DN | DDIC_TXC(1)                              |
|        | DDIC_TXC4                                      | HDMIc_TX0_DP | DDIC_TXC(2)                              |
|        | DDIC_TXC5                                      | HDMIc_TX0_DN | DDIC_TXC(2)                              |
|        | DDIC_TXC6                                      | HDMIc_CLK_DP | DDIC_TXC(3)                              |
|        | DDIC_TXC7                                      | HDMIc_CLK_DN | DDIC_TXC(3)                              |
|        | DDIC_TXC8                                      | HDMIc_CLK_DP | DDIC_TXC(3)                              |
|        | DDIC_TXC9                                      | HDMIc_CLK_DN | DDIC_TXC(3)                              |
| Port D | DDID_TXD0                                      | HDMIb_TX2_DP | DDID_TXD(0)                              |
|        | DDID_TXD1                                      | HDMIb_TX2_DN | DDID_TXD(0)                              |
|        | DDID_TXD2                                      | HDMIb_TX1_DP | DDID_TXD(1)                              |
|        | DDID_TXD3                                      | HDMIb_TX1_DN | DDID_TXD(1)                              |
|        | DDID_TXD4                                      | HDMIb_TX0_DP | DDID_TXD(2)                              |
|        | DDID_TXD5                                      | HDMIb_TX0_DN | DDID_TXD(2)                              |
|        | DDID_TXD6                                      | HDMIb_CLK_DP | DDID_TXD(3)                              |
|        | DDID_TXD7                                      | HDMIb_CLK_DN | DDID_TXD(3)                              |
|        | DDID_TXD8                                      | HDMIb_CLK_DP | DDID_TXD(3)                              |
|        | DDID_TXD9                                      | HDMIb_CLK_DN | DDID_TXD(3)                              |



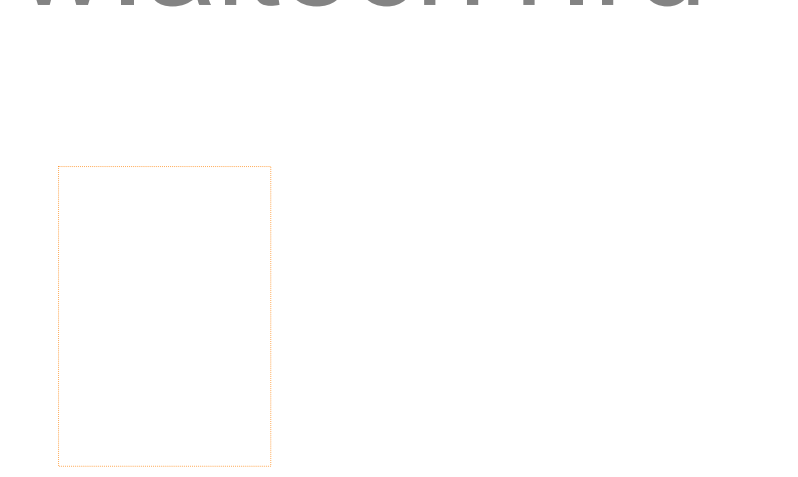
PDG P132

HSW A0+LPT A0 change R21to 4.7K, R19 to 3.3K

Trace width=12mil, spacing 20mil, max L=500mil



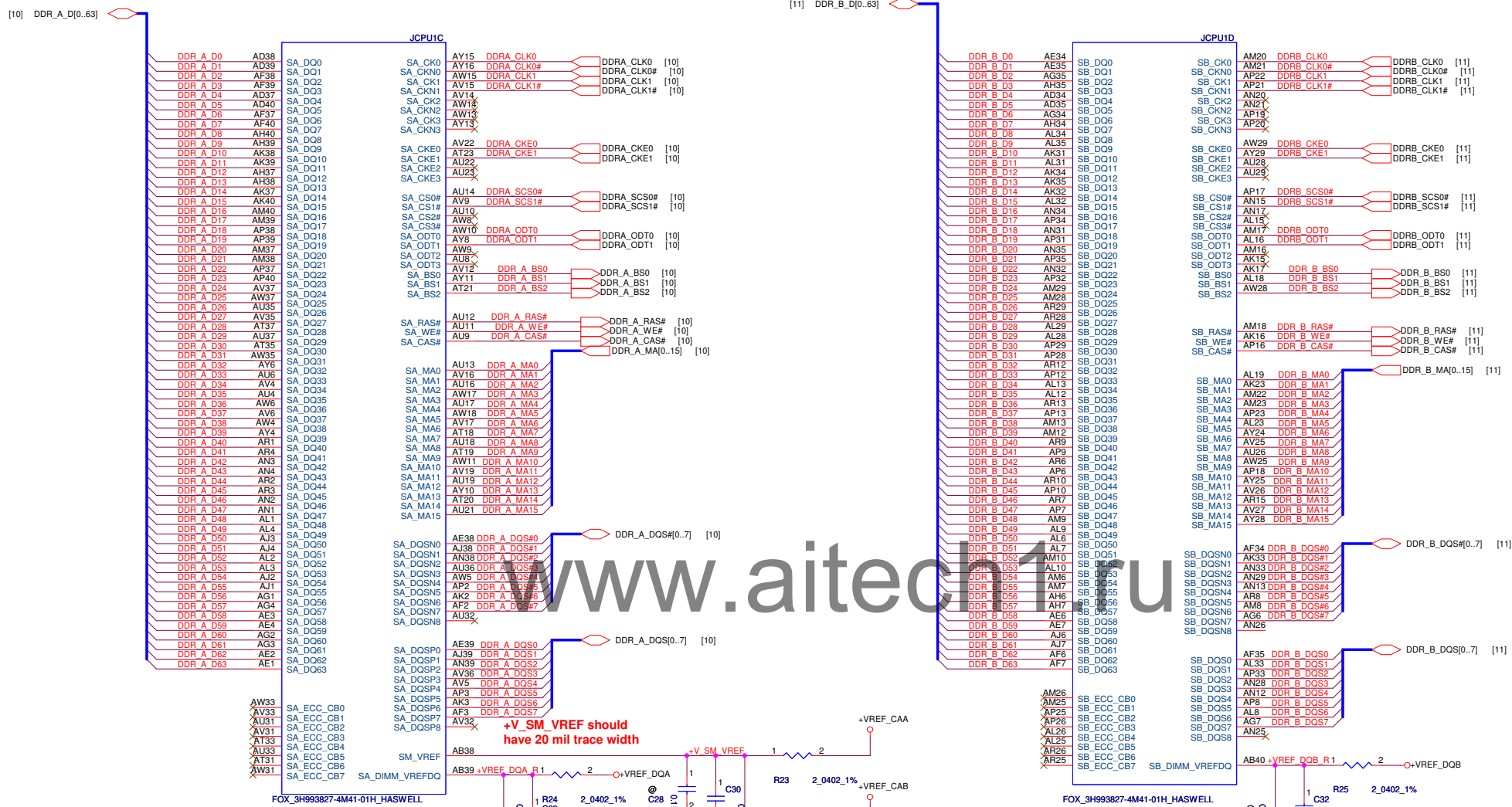
FOX\_3H93827-4M41-01H\_HASWELL



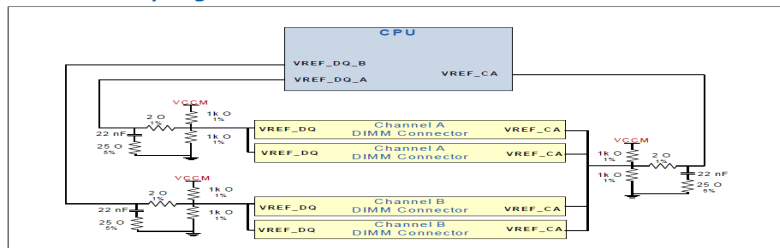
v0.2 update

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| Size  | Document Number    | Rev             | Date: Tuesday, September 24, 2013 Sheet 5 of 59 |                      |
| Custom  | ZEAA0 LA-A061P M/B | 0.3             |   |                      |





DDR3 VREF Topologies

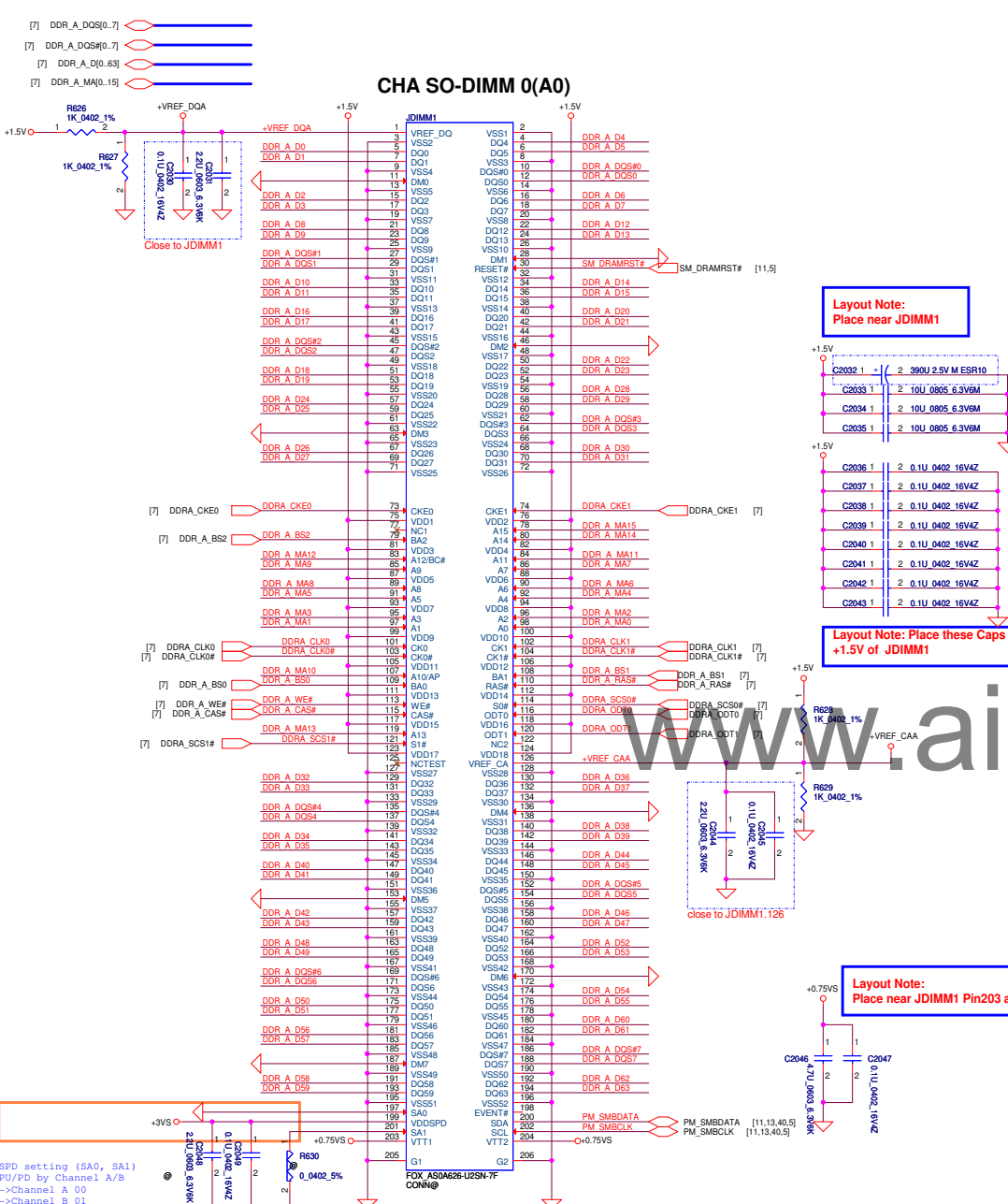


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| Title   | Haswell DDR3                |                 |                          |         |
| Size  | Custom                      | Document Number | ZEAA0 LA-A061P M/B       | Rev 0.3 |
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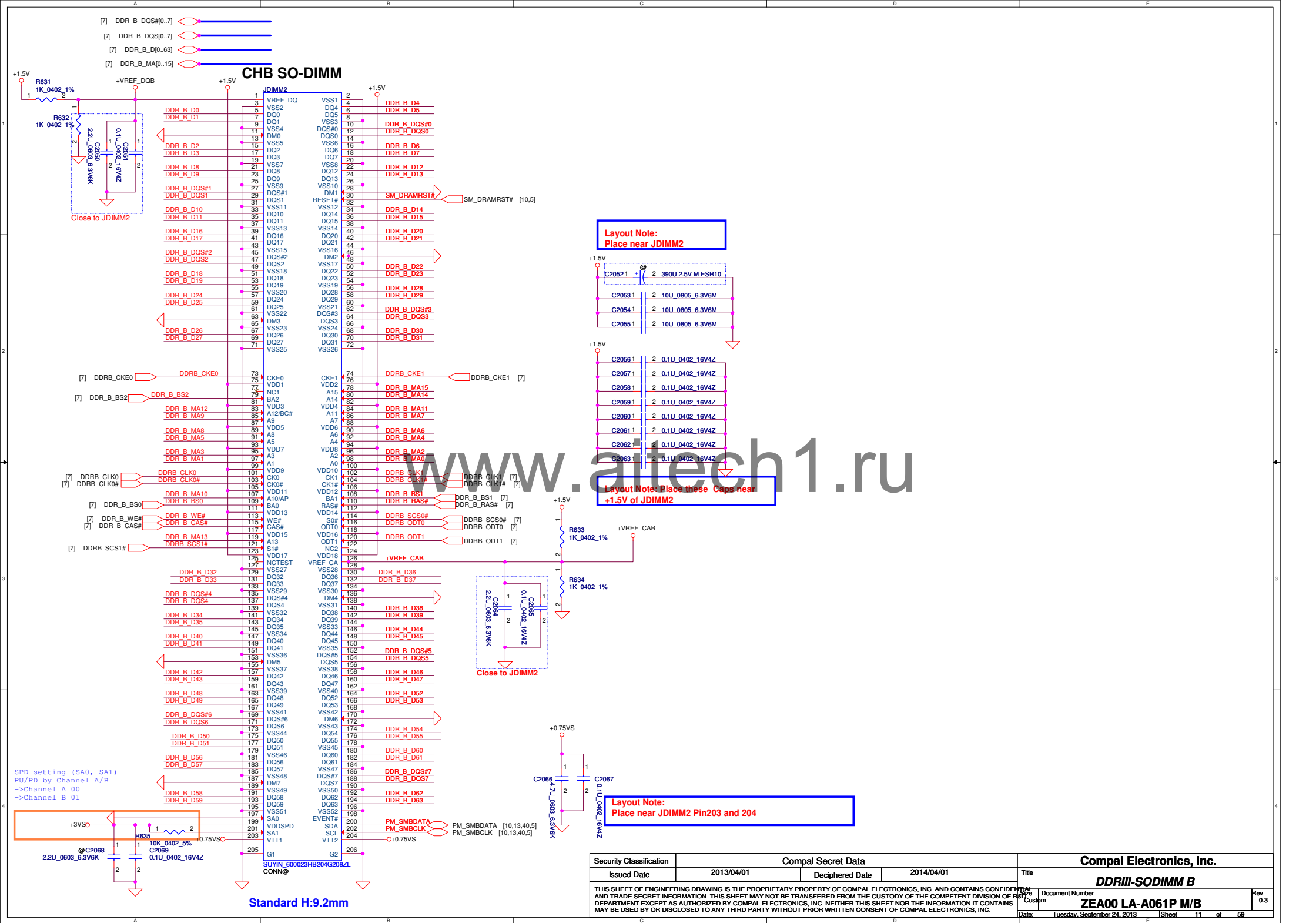






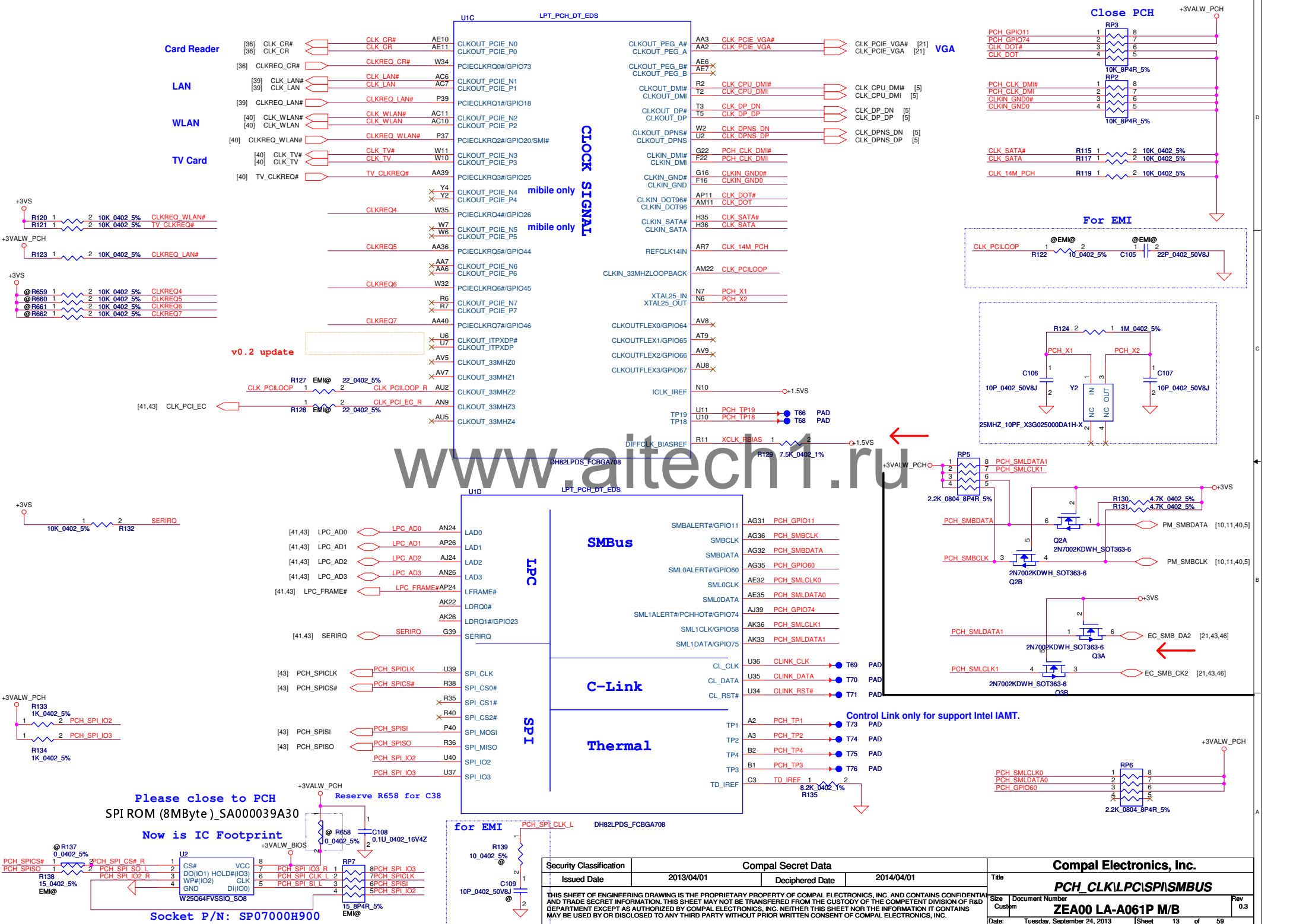
**Layout Note:**  
Place near J10MM1, Pin 200 and 204

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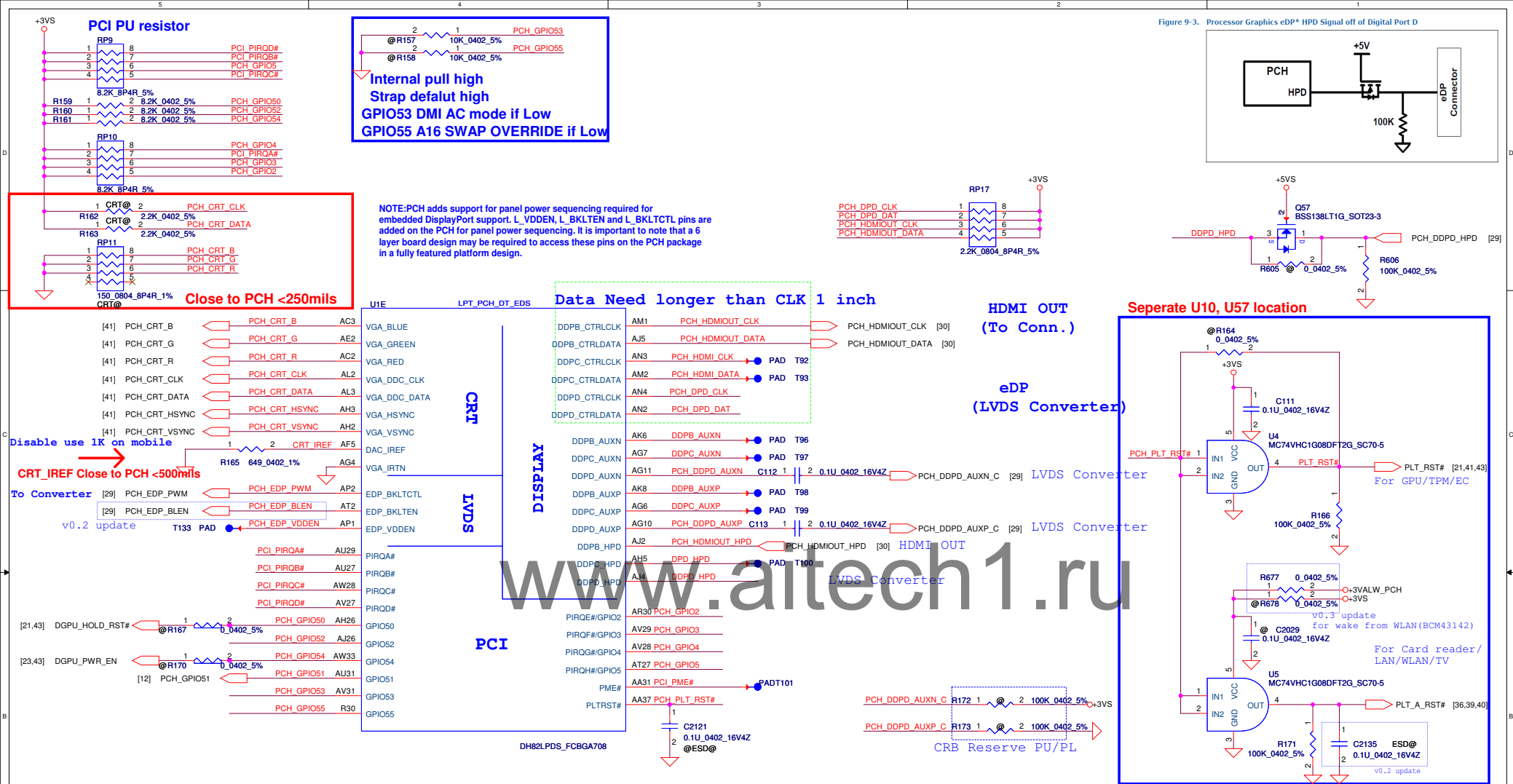
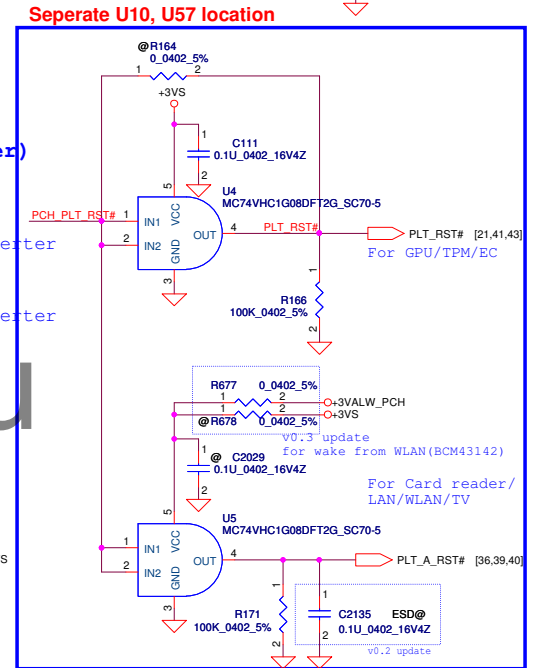
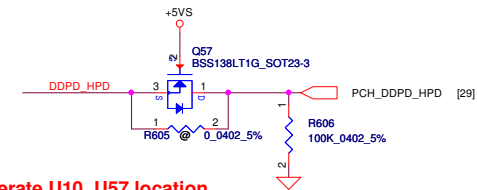
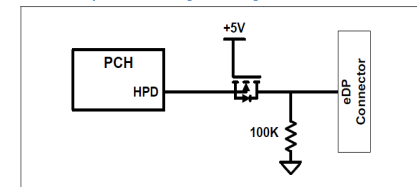
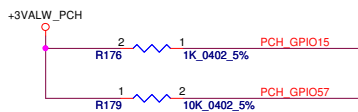


Figure 9-3. Processor Graphics eDP\* HPD Signal off of Digital Port D



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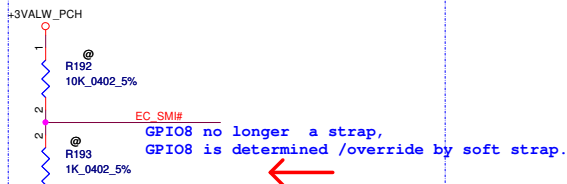




#### GPIO8

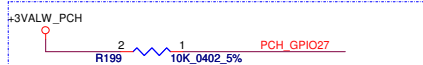
Integrated Clock Chip Enable (Removed)

H: Disable  
L: Enable



This signal has a weak internal pull-up but requires an external pull down.

The current default is clock enable



In Deep Sleep Power Well. Unmuxed. Defaults to GPI. Not used Weak pull-up 10kΩ to VccDSW3\_3 -->Check list1.5 P402. PD to GND for Huron River!!

#### GPIO28

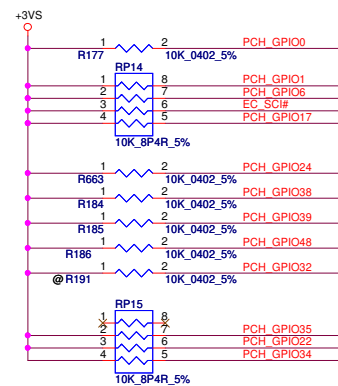
On-Die PLL Voltage Regulator

H: Enable  
L: Disable



Clock validation strap  
ICG is EN when LOW  
\*GPIO36 with internal pull-down

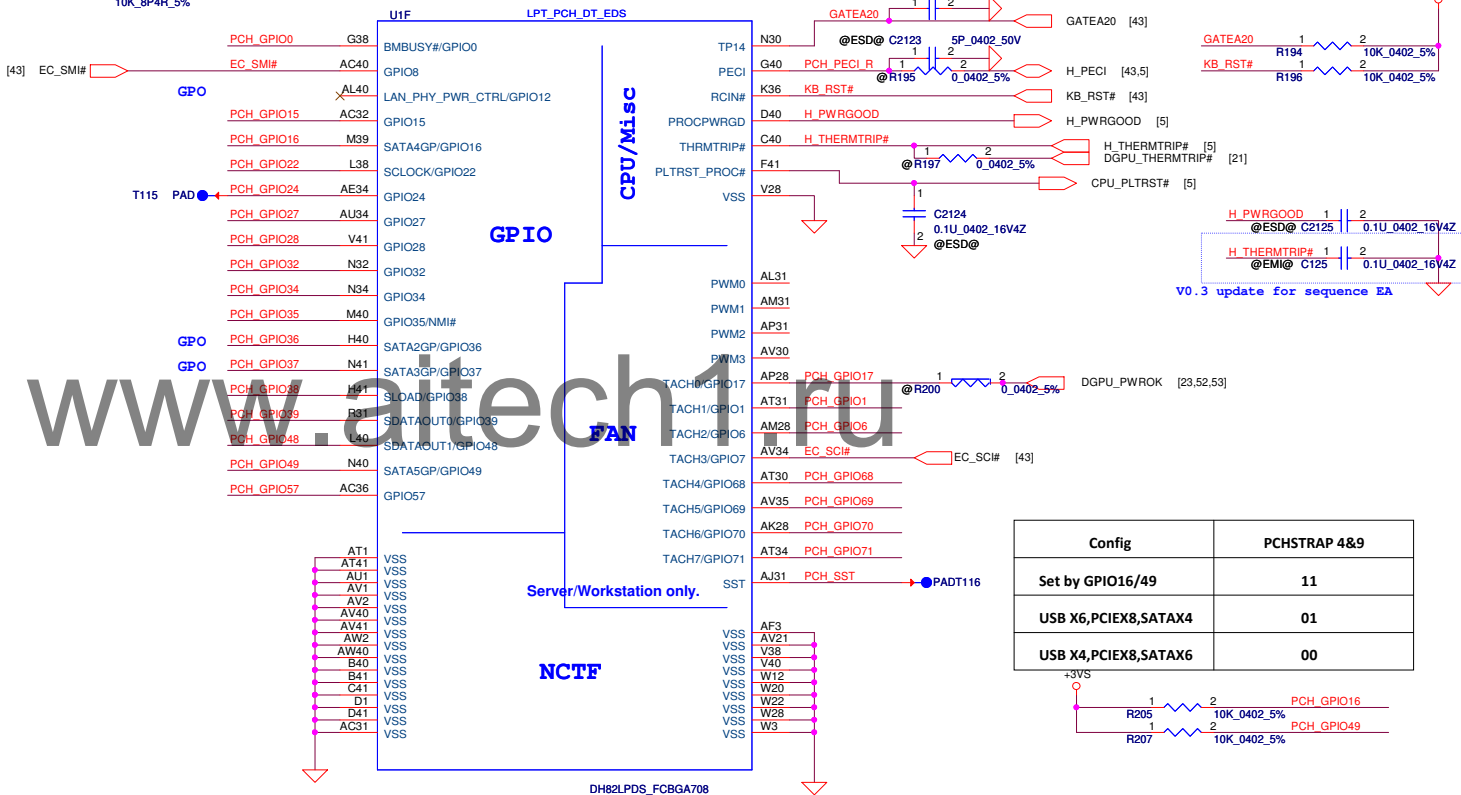
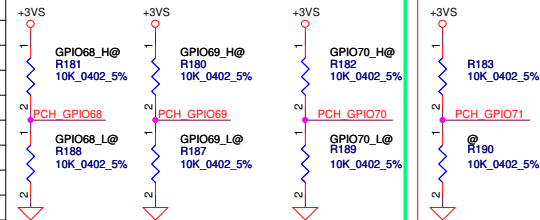
TL5  
Hi:with confidentiality  
Low:with no confidentiality  
\*GPIO37 with internal pull-down



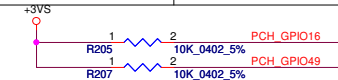
120821

| SKU ID | GPIO68 | GPIO69 | GPIO69 |
|--------|--------|--------|--------|
| SKU1   | 0      | 0      | 0      |
| SKU2   | 0      | 0      | 1      |
| SKU3   | 0      | 1      | 0      |
| SKU4   | 0      | 1      | 1      |
| SKU5   | 1      | 0      | 0      |
| SKU6   | 1      | 0      | 1      |
| SKU7   | 1      | 1      | 0      |
| SKU8   | 1      | 1      | 1      |

SKU ID TABLE

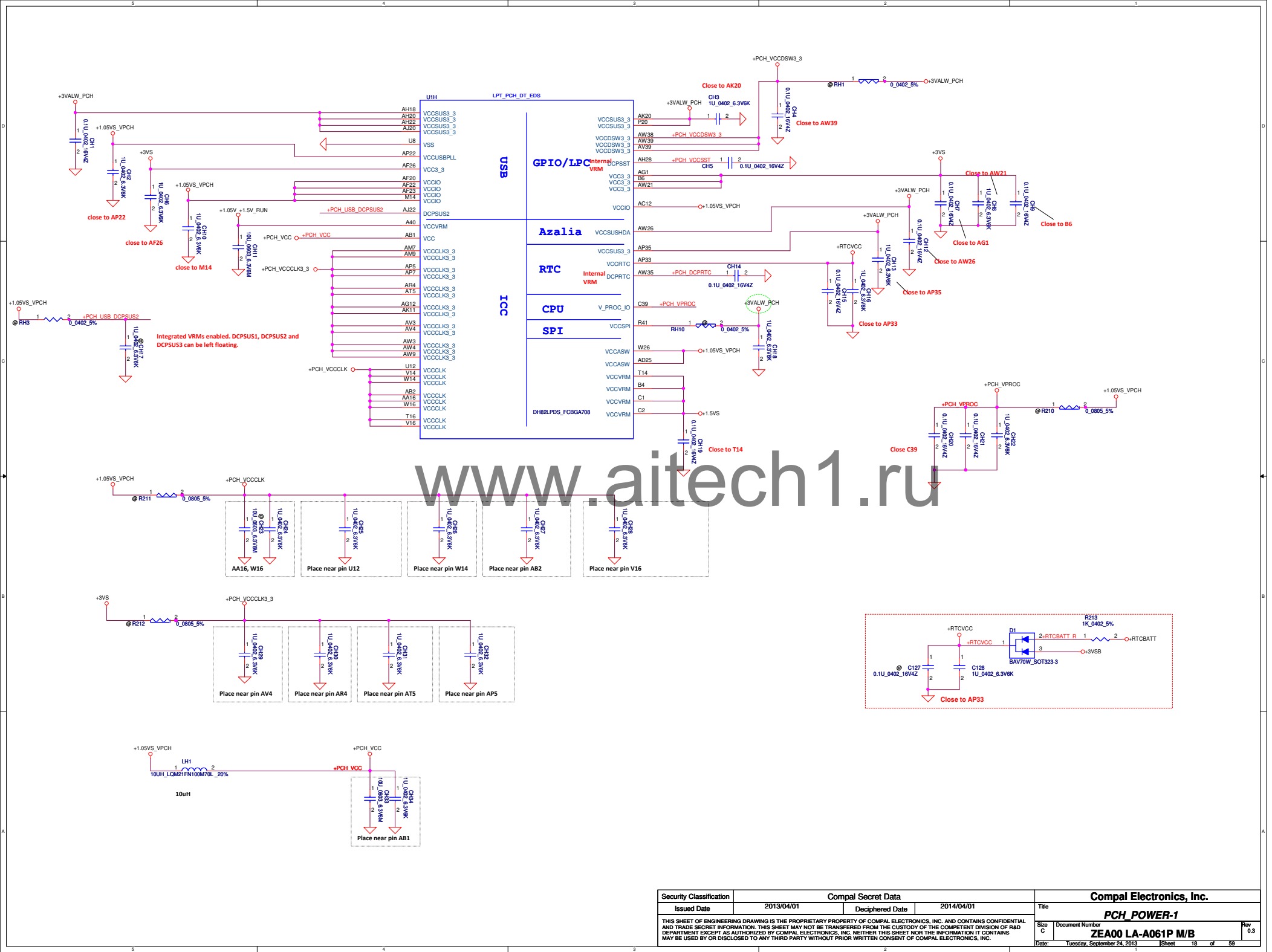


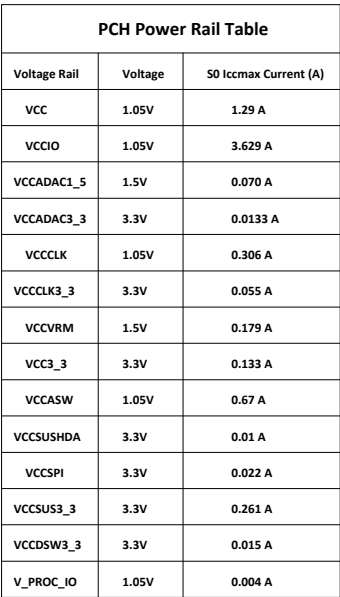
| Config               | PCHSTRAP 4&9 |
|----------------------|--------------|
| Set by GPIO16/49     | 11           |
| USB X6,PCIEX8,SATAx4 | 01           |
| USB X4,PCIEX8,SATAx6 | 00           |



| Fixed Signals |           |           |           | Muxed Signals |           | Fixed Signals |           |           |           |           |           | Muxed Signals |           | Fixed Signals |           |           |           |
|---------------|-----------|-----------|-----------|---------------|-----------|---------------|-----------|-----------|-----------|-----------|-----------|---------------|-----------|---------------|-----------|-----------|-----------|
| USB3<br>1     | USB3<br>2 | USB3<br>5 | USB3<br>6 | PCIE<br>1     | PCIE<br>2 | PCIE<br>3     | PCIE<br>4 | PCIE<br>5 | PCIE<br>6 | PCIE<br>7 | PCIE<br>8 | SATA<br>4     | SATA<br>5 | SATA<br>0     | SATA<br>1 | SATA<br>2 | SATA<br>3 |
|               |           |           |           | (00)          | (00)      |               |           |           |           |           |           | (00)          | (00)      |               |           |           |           |
|               |           |           |           | USB3<br>3     | USB3<br>4 |               |           |           |           |           |           | PCIE<br>1     | PCIE<br>2 |               |           |           |           |

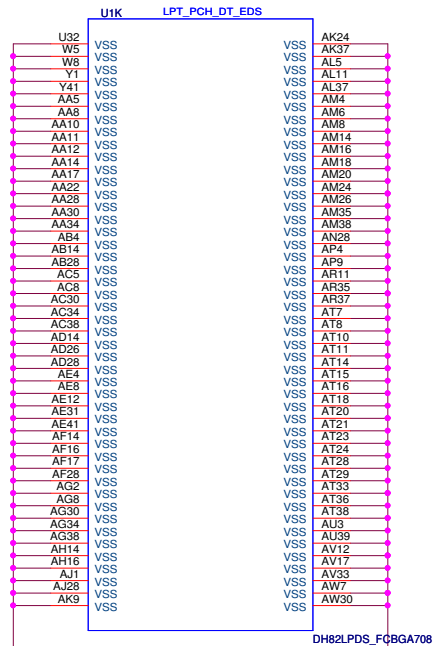
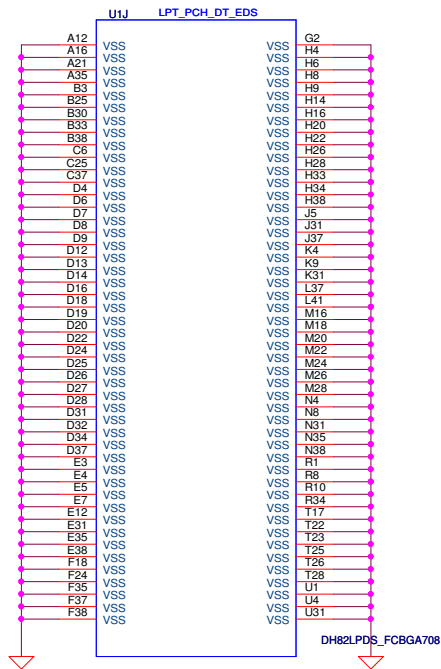
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| PCH Power Rail Table |         |                       |
|----------------------|---------|-----------------------|
| Voltage Rail         | Voltage | S0 Iccmax Current (A) |
| VCC                  | 1.05V   | 1.29 A                |
| VCCIO                | 1.05V   | 3.629 A               |
| VCCADACL_5           | 1.5V    | 0.070 A               |
| VCCADAC3_3           | 3.3V    | 0.0133 A              |
| VCCCLK               | 1.05V   | 0.306 A               |
| VCCCLK3_3            | 3.3V    | 0.055 A               |
| VCCVRM               | 1.5V    | 0.179 A               |
| VCC3_3               | 3.3V    | 0.133 A               |
| VCCASW               | 1.05V   | 0.67 A                |
| VCCSUSHDA            | 3.3V    | 0.01 A                |
| VCCSPI               | 3.3V    | 0.022 A               |
| VCCSUS3_3            | 3.3V    | 0.261 A               |
| VCCDSW3_3            | 3.3V    | 0.015 A               |
| V_PROC_IO            | 1.05V   | 0.004 A               |





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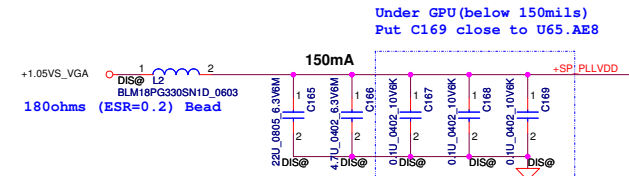
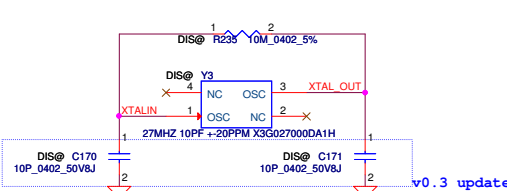
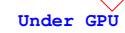
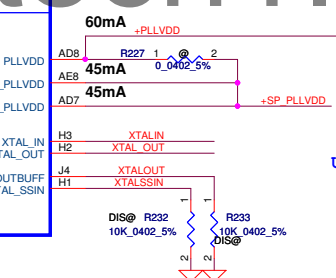
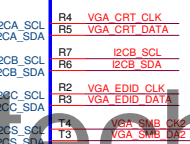
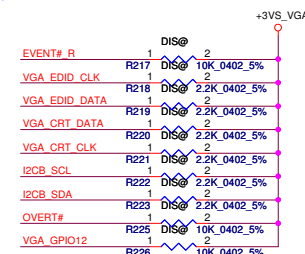
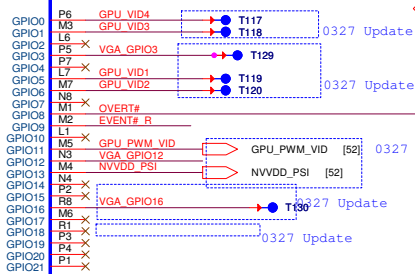
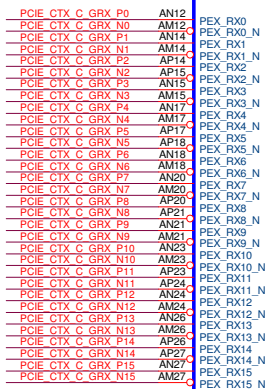
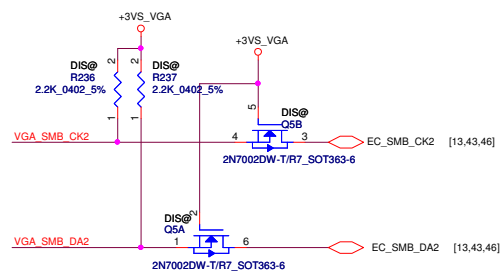
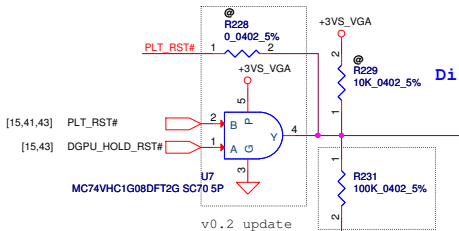
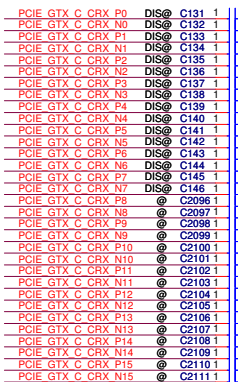
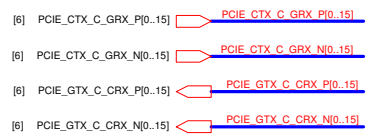


Table 102. GB2-64 and GB4-128 GPIO Description

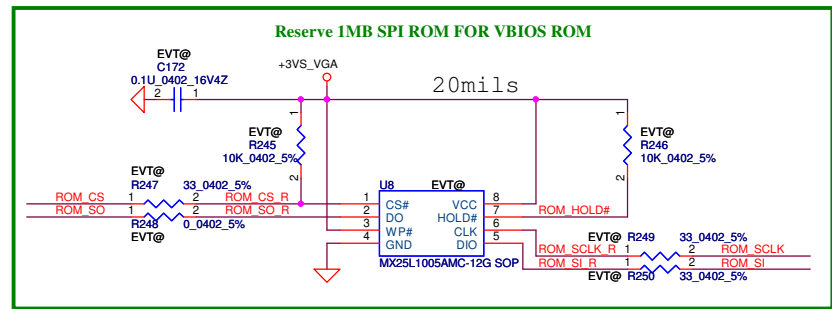
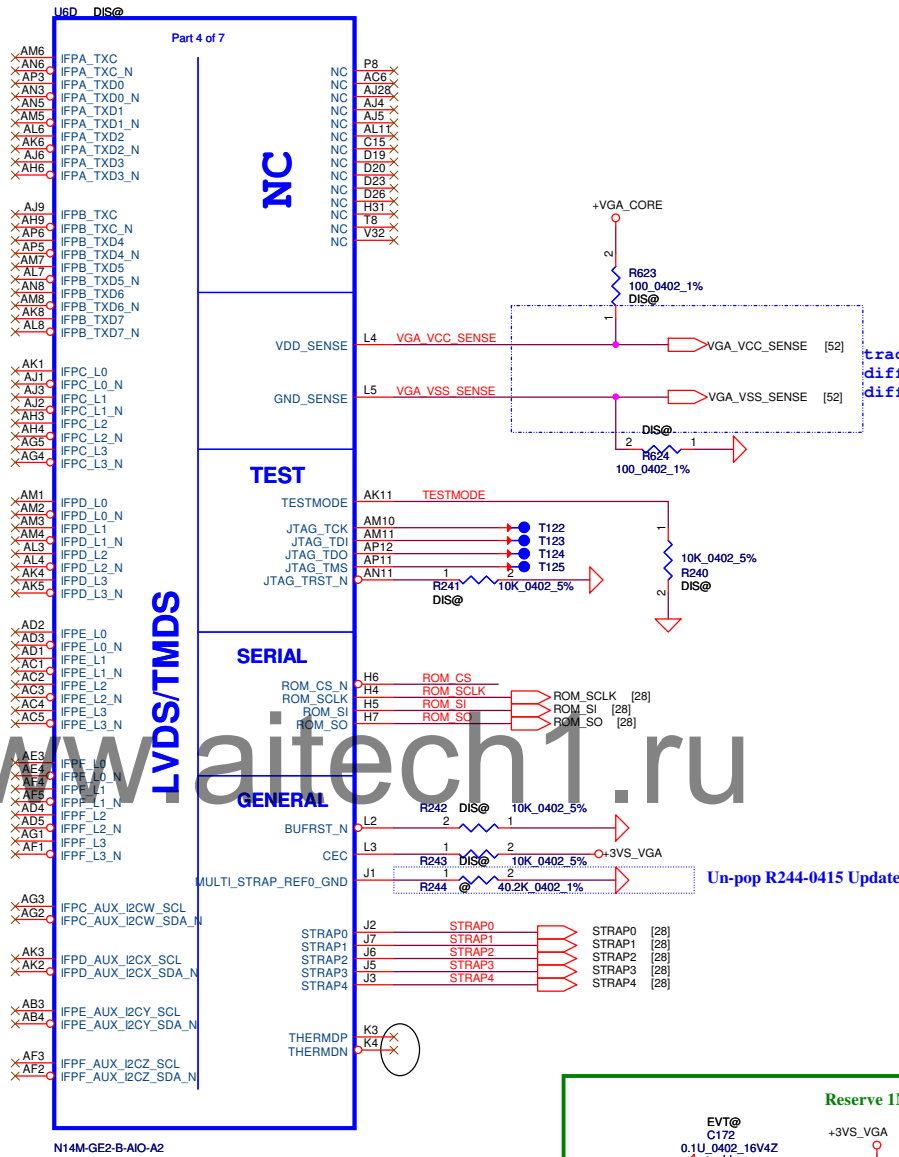
| GPIO pin Name | Normal Function    | I/O | Functional Description                           | Recommended Default Pull-up or Pull-down  |
|---------------|--------------------|-----|--|---|
| GPIO0         | GPIO_VID4          | 0   | GPU Core VDD VID4                                | Strap to boot HVVDD   |
| GPIO1         | GPIO_VID3          | 0   | GPU Core VDD VID3                                | Strap to boot HVVDD   |
| GPIO2         | LCD_BLK_PWM        | 0   | Panel Backlight PWM Brightness Control           | 100 K pull-down   |
| GPIO3         | LCD_VCC or PSI     | 0   | Panel Power Enable or Phase Sheddng              | LCD_VCC: 100k pull-down<br>PSI: 10k pull-up or pull-down; stuff as needed to disable phase shedding by default            |
| GPIO4         | LCD_BEN1           | 0   | Panel Backlight Enable                           | 100 K pull-down   |
| GPIO5         | GPU_VID1           | 0   | GPU Core VDD VID1                                | Strap to boot HVVDD   |
| GPIO6         | GPU_VID2           | 0   | GPU Core VDD VID2                                | Strap to boot HVVDD   |
| GPIO7         | 3Dvision           | 0   | 3D Vision Left/Right signal                      | 100 K pull-down   |
| GPIO8         | OVERT              | I/O | Active Low Thermal Catastrophic Over Temperature | 100 K pull-up   |
| GPIO9         | ALERT              | I/O | Active Low Thermal Alert                         | 100 K pull-up   |
| GPIO10        | MEM_VREF_CTL       | 0   | Memory VREF Control                              | 100 K pull-down   |
| GPIO11        | GPU_VID0           | 0   | GPU Core VDD VID0                                | Strap to boot HVVDD   |
| GPIO12        | PWR_LEVEL          | I   | AC power detect or power supply overdraw input   | 100 K pull-up   |
| GPIO13        | GPU_VID5           | 0   | GPU Core VDD VID5                                | Strap to boot HVVDD   |
| GPIO14        | HPD_AB             | I   | Hot Plug Detect for IPFAB                        | See Figure 76   |
| GPIO15        | HPD_C              | I   | Hot Plug Detect for IPFC                         | See Figure 76   |
| GPIO16        | PSI or MEM_VDD_CTL | 0   | Phase Sheddng or Memory VDD VID                  | PSI: 10k pull-up or pull-down; stuff as needed to disable phase shedding by default<br>MEM_VDD_CTL: Strap to boot FBVDD_Q |
| GPIO17        | HPD_D              | I   | Hot Plug Detect for IPFD                         | See Figure 76   |
| GPIO18        | HPD_E              | I   | Hot Plug Detect for IPFE                         | See Figure 76   |
| GPIO19        | HPD_F              | I   | Hot Plug Detect for IPFF                         | See Figure 76   |
| GPIO20        | Reserved           |     |  |   |
| GPIO21        | Reserved           |     |  |   |

Reserve pull-up and down.  
Don't have to install  
component for default, NV  
reply on 5/4. when system  
no support CLKREQ

|   |  |                    |  |                 |  |                                 |  |                             |  |                           |  |       |  |
|---|--|--------------------|--|-----------------|--|---------------------------------|--|-----------------------------|--|---------------------------|--|-------|--|
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|   |  |                    |  |                 |  | Size                            |  | Document Number             |  | <b>ZEA00 LA-A061P M/B</b> |  | Rev.3 |  |
|   |  |                    |  |                 |  | Date:                           |  | Tuesday, September 24, 2013 |  |                           |  |       |  |
|   |  |                    |  |                 |  |                                 |  |                             |  | Sheet 21 of 59            |  |       |  |

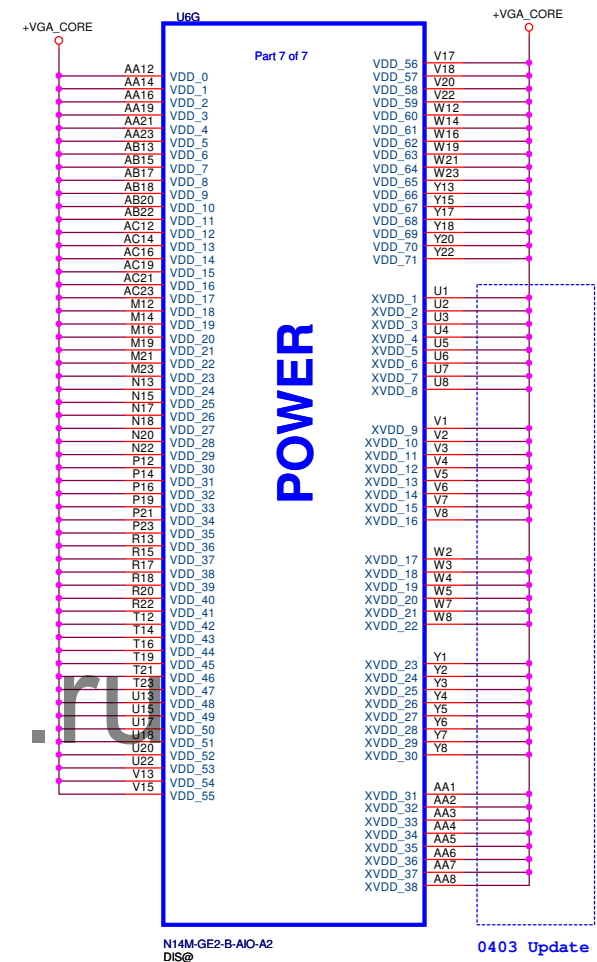
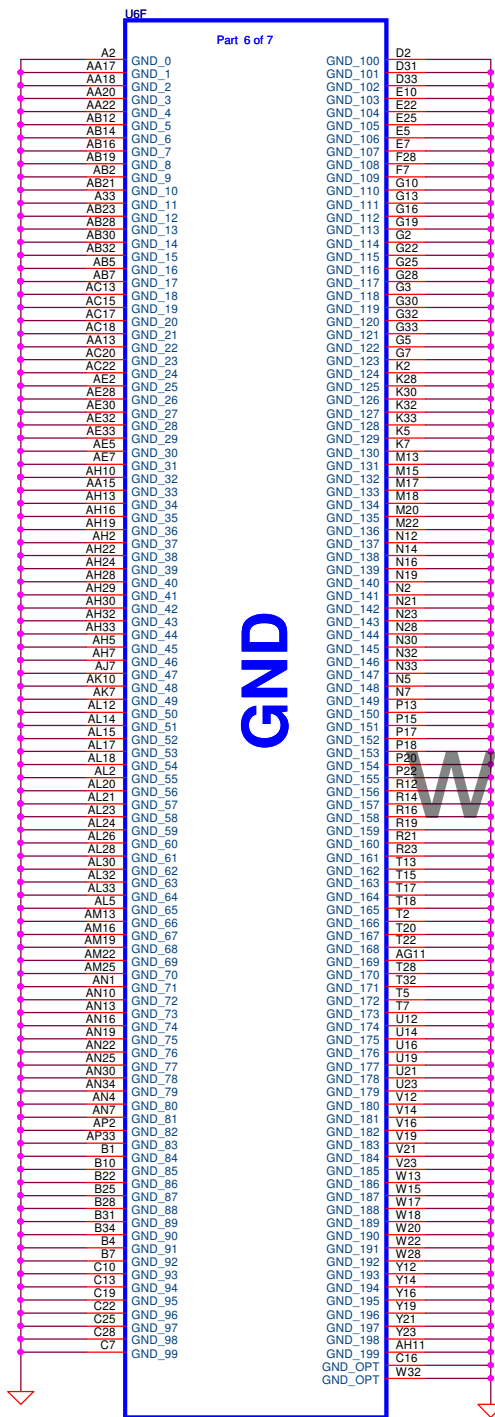
Table 66. N13x Family Display Link Summary

| Link   | Description   |
|--------|---|
| Link A | LVDS (Single Link or Dual Link with IFPB)                         |
| Link B | LVDS (Dual Link with IFPA)  |
| Link C | DisplayPort,<br>HDMI  |
| Link D | DisplayPort,<br>eDP   |
| Link E | DisplayPort,<br>DVI (Single Link or Dual Link with IFPF),<br>HDMI |
| Link F | DisplayPort,<br>DVI (Dual Link with IFPE),<br>HDMI                |



|   |            |                    |            |   |                             |                |
|---|------------|--------------------|------------|---|-----------------------------|----------------|
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| Issued Date   | 2013/04/01 | Deciphered Date    | 2014/04/01 | Title   |                             |                |
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|   |            |                    |            |   | <b>ZEA00 LA-A061P M/B</b>   | 0.3            |
|   |            |                    |            | Date:   | Tuesday, September 24, 2013 | Sheet 22 of 59 |



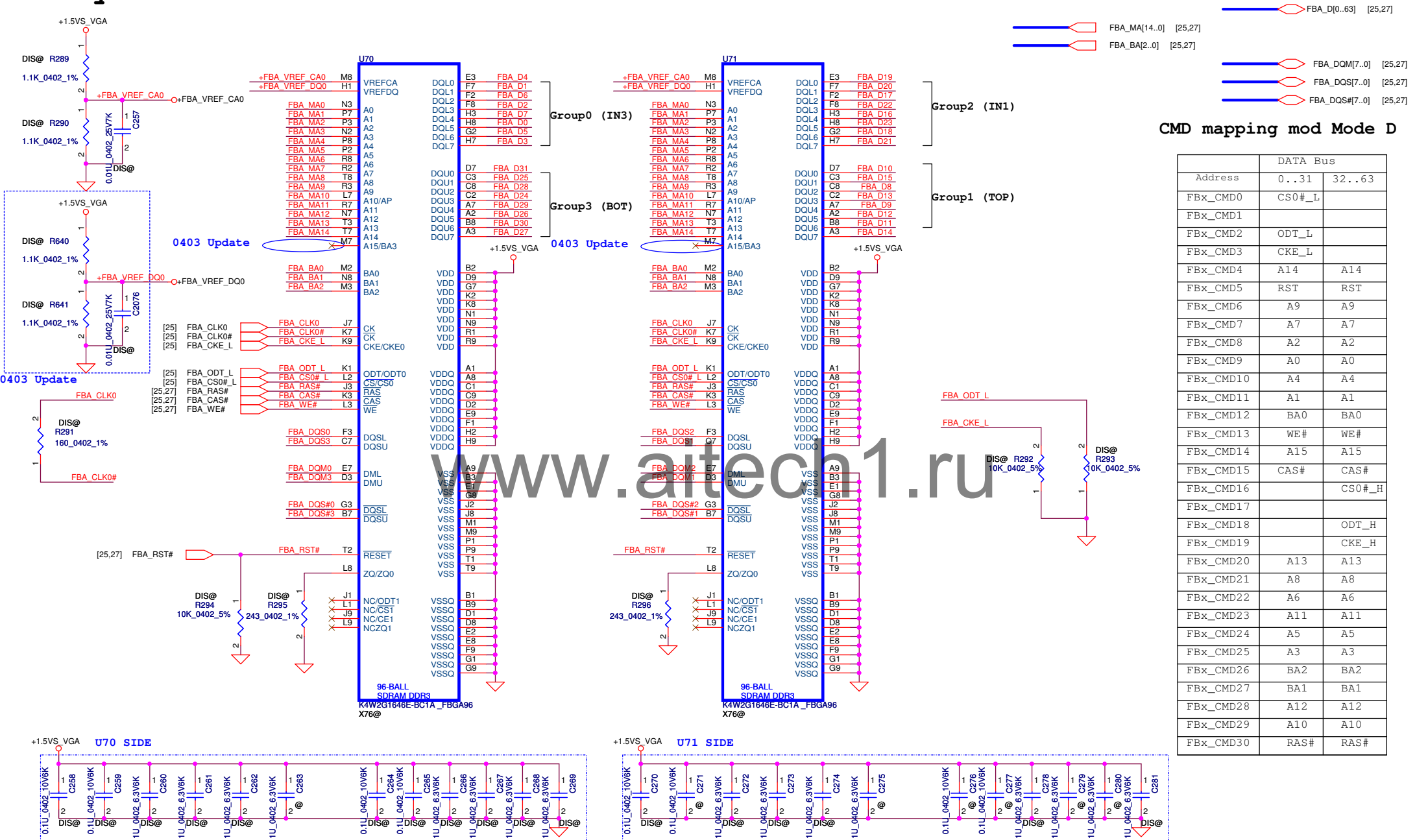


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| Issued Date   |  | 2013/04/01         |  | Deciphered Date          |  | 2014/04/01 |  | Title                       |  |                |  |  |  |  |  |  |  |
|   |  |                    |  |                          |  |            |  | N14M-GE2-VGA CORE, GND      |  |                |  |  |  |  |  |  |  |
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| Size  |  |                    |  |                          |  |            |  | Document Number             |  | Rev            |  |  |  |  |  |  |  |
|   |  |                    |  |                          |  |            |  | ZEA00 LA-A061P M/B          |  | 0.3            |  |  |  |  |  |  |  |
|   |  |                    |  |                          |  | Date:      |  | Tuesday, September 24, 2013 |  | Sheet 24 of 59 |  |  |  |  |  |  |  |



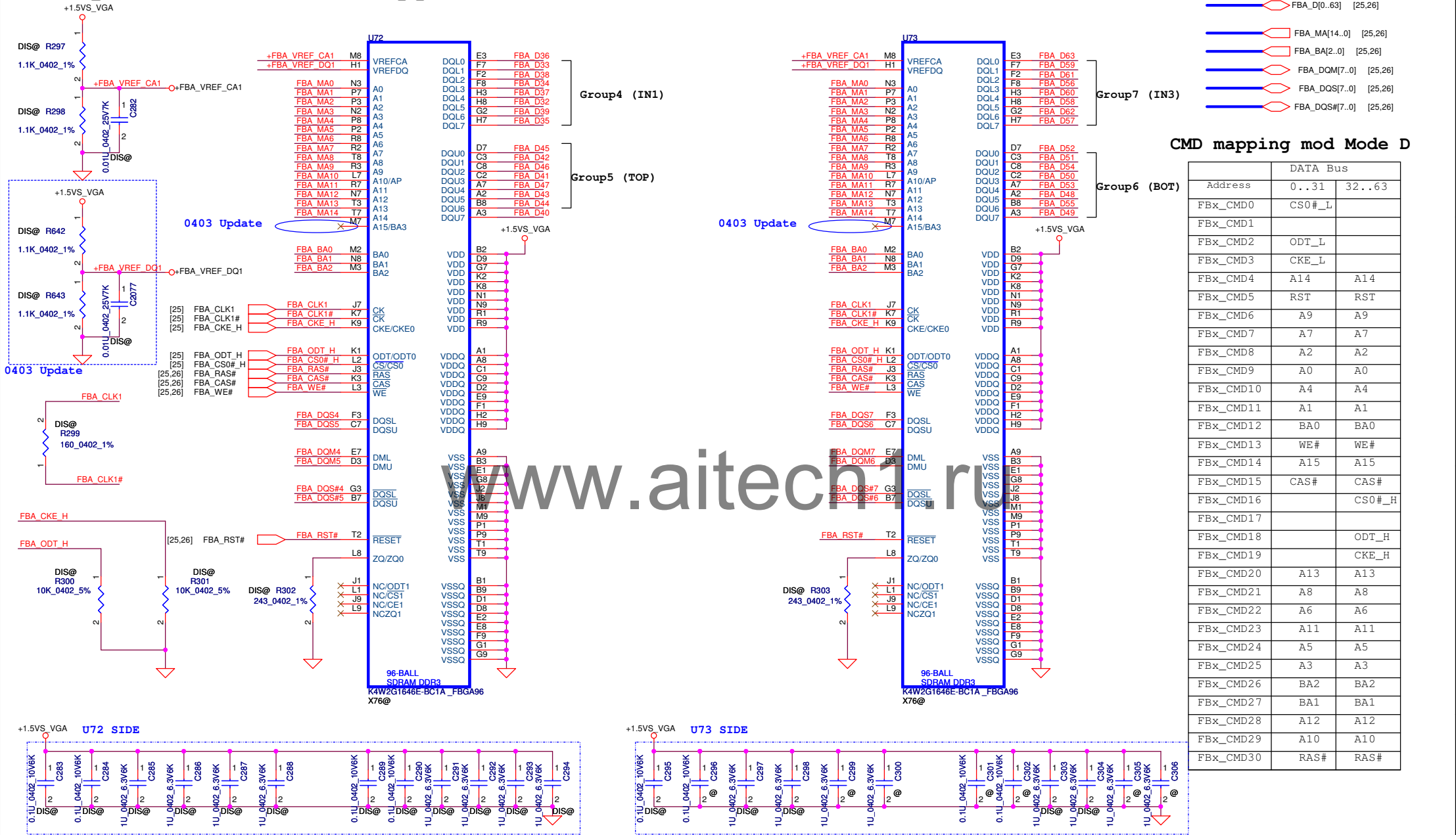


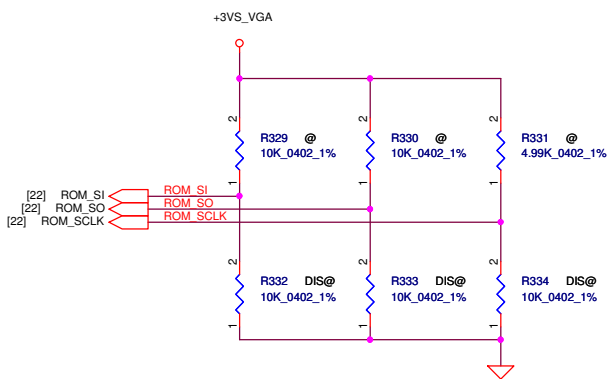
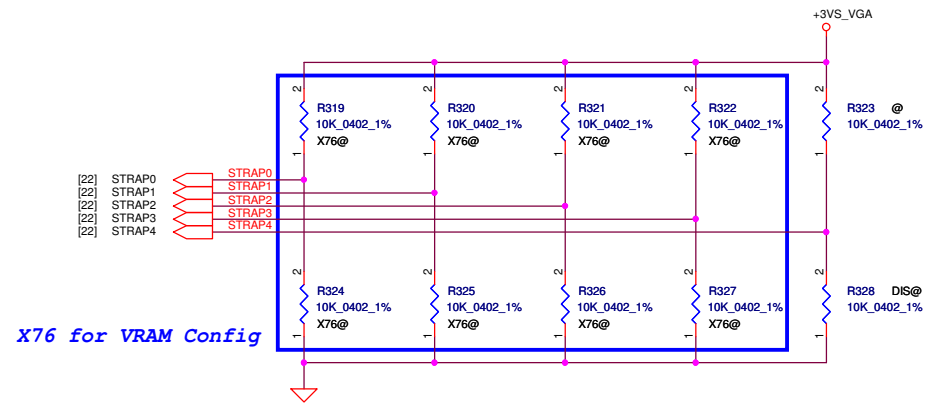
## Memory Partition A - Lower 32 bits



|           | DATA Bus |        |
|-----------|----------|--------|
| Address   | 0..31    | 32..63 |
| FBx_CMD0  | CS0#_L   |        |
| FBx_CMD1  |          |        |
| FBx_CMD2  | ODT_L    |        |
| FBx_CMD3  | CKE_L    |        |
| FBx_CMD4  | A14      | A14    |
| FBx_CMD5  | RST      | RST    |
| FBx_CMD6  | A9       | A9     |
| FBx_CMD7  | A7       | A7     |
| FBx_CMD8  | A2       | A2     |
| FBx_CMD9  | A0       | A0     |
| FBx_CMD10 | A4       | A4     |
| FBx_CMD11 | A1       | A1     |
| FBx_CMD12 | BA0      | BA0    |
| FBx_CMD13 | WE#      | WE#    |
| FBx_CMD14 | A15      | A15    |
| FBx_CMD15 | CAS#     | CAS#   |
| FBx_CMD16 |          | CS0#_  |
| FBx_CMD17 |          |        |
| FBx_CMD18 |          | ODT_H  |
| FBx_CMD19 |          | CKE_H  |
| FBx_CMD20 | A13      | A13    |
| FBx_CMD21 | A8       | A8     |
| FBx_CMD22 | A6       | A6     |
| FBx_CMD23 | A11      | A11    |
| FBx_CMD24 | A5       | A5     |
| FBx_CMD25 | A3       | A3     |
| FBx_CMD26 | BA2      | BA2    |
| FBx_CMD27 | BA1      | BA1    |
| FBx_CMD28 | A12      | A12    |
| FBx_CMD29 | A10      | A10    |
| FBx_CMD30 | RAS#     | RAS#   |

Memory Partition A - Upper 32 bits





[PUN-06026-001]

Table 4. Binary Strap Mode Mapping

| Strap Pin Name | Strap Mapping  | Resistance   | Polarity   |
|----------------|----------------|--------------|--|
| ROM_SCLK       | SMB_ALT_ADDR   | 10k $\Omega$ | Pull-down to GND   |
| ROM_SI         | SUB_VENDOR     | 10k $\Omega$ | Pull-up to 3V3 if VBIOS ROM exists<br>Pull-down to GND if no VBIOS ROM |
| ROM_SO         | VGA_DEVICE     | 10k $\Omega$ | Pull-down to GND (no display)  |
| STRAP0         | RAM_CFG[0]     | 10k $\Omega$ | See Note   |
| STRAP1         | RAM_CFG[1]     | 10k $\Omega$ | See Note   |
| STRAP2         | RAM_CFG[2]     | 10k $\Omega$ | See Note   |
| STRAP3         | RAM_CFG[3]     | 10k $\Omega$ | See Note   |
| STRAP4         | PCIE_MAX_SPEED | 10k $\Omega$ | Pull-down to GND   |

[VRAM Config-RVL-06366-001]

| GPU      | Freq.   | Memory Size        | Memory Config                                       | strap3              | strap2              | strap1              | strap0              |
|----------|---------|--------------------|---|---------------------|---------------------|---------------------|---------------------|
| N14M-GE2 | 900 MHz | 128M* 16* 4<br>1GB | Hynix (0x6)<br>H5TQ2G63BFR-11C<br>SA00003YO10       | 0<br>R327<br>PD 10K | 1<br>R321<br>PU 10K | 1<br>R320<br>PU 10K | 0<br>R324<br>PD 10K |
|          |         |                    | Samsung (0x5)<br>K4W2G1646E-BC11<br>SA00005SH00     | 0<br>R327<br>PD 10K | 1<br>R321<br>PU 10K | 0<br>R325<br>PD 10K | 1<br>R319<br>PU 10K |
|          |         |                    | Micron (0x1)<br>MT41J128M16JT-107G:K<br>SA00005SM30 | 0<br>R327<br>PD 10K | 0<br>R326<br>PD 10K | 0<br>R325<br>PD 10K | 1<br>R319<br>PU 10K |
| N14M-GE2 | 900 MHz | 256M* 16* 4<br>2GB | Micron (0xD)<br>MT41K256M16HA-107G:E<br>SA00006SD20 | 1<br>R322<br>PU 10K | 1<br>R321<br>PU 10K | 0<br>R325<br>PD 10K | 1<br>R319<br>PU 10K |
|          |         |                    | Samsung (0xB)<br>K4W4G1646B-HC11<br>SA000068R10     | 1<br>R322<br>PU 10K | 0<br>R326<br>PD 10K | 1<br>R320<br>PU 10K | 1<br>R319<br>PU 10K |
|          |         |                    | Hynix (0x4)<br>H5TC4G63AFR-11C<br>SA00006E800       | 0<br>R327<br>PD 10K | 1<br>R321<br>PU 10K | 0<br>R325<br>PD 10K | 0<br>R324<br>PD 10K |

|   |  |                    |  |                 |  |                                 |  |                             |  |                |  |
|---|--|--------------------|--|-----------------|--|---------------------------------|--|-----------------------------|--|----------------|--|
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|   |  |                    |  |                 |  | Date:                           |  | Tuesday, September 24, 2013 |  | Sheet 28 of 59 |  |
|   |  |                    |  |                 |  |                                 |  |                             |  |                |  |



## Power Consumption:

Pin 22 (PVCC) < 50 mA

Pin 18 (SWR\_VDD) < 200mA (layout trace > 40 mil)

Pin5 (DPV33) < 20mA

Pin 17 (SWR\_LX) < 600mA (layout trace > 60 mil)

Pin 15 (SWR\_VCCK) < 100mA (layout trace > 60 mil)

Pin 43 (VCCK) < 50mA

Pin 11 (DPV12) < 100mA

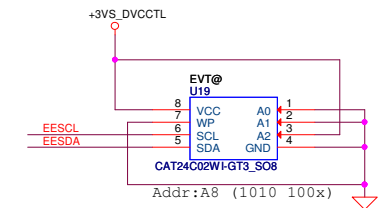
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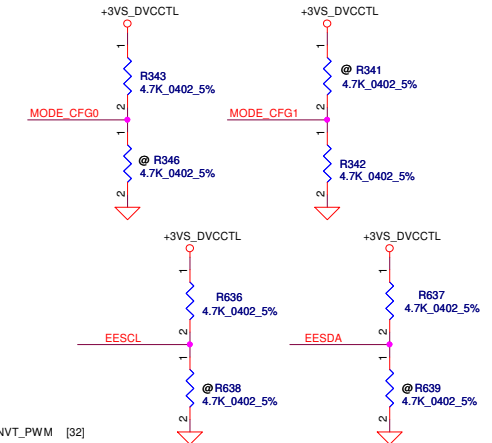
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v0.2 update

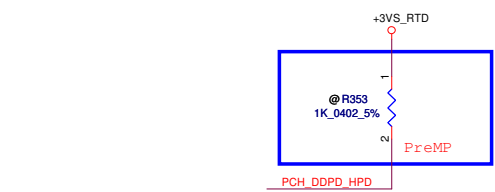
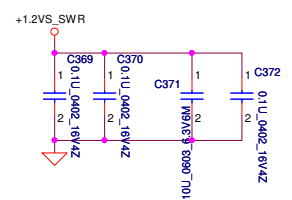
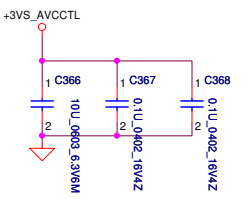
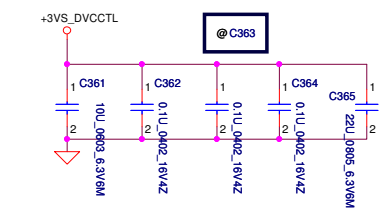
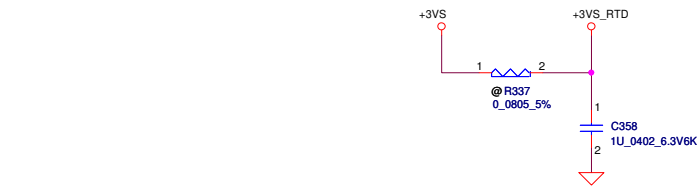
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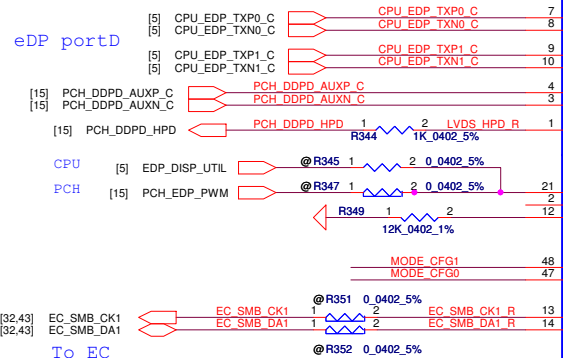
EVT Debug Only, un-pop for DVT



| Pin 47 |   |     |         |
|--------|---|-----|---------|
|        | 0 | 1   |         |
| Pin 48 | 0 | X   | EP Mode |
|        | 1 | ROM | EEPROM  |

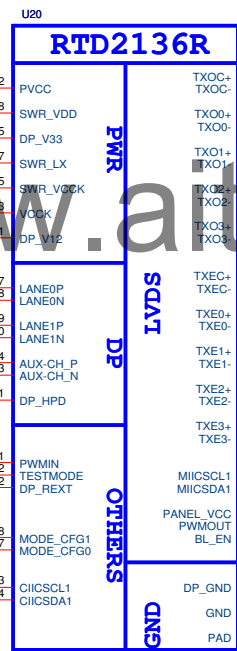


## eDP portD



To EC

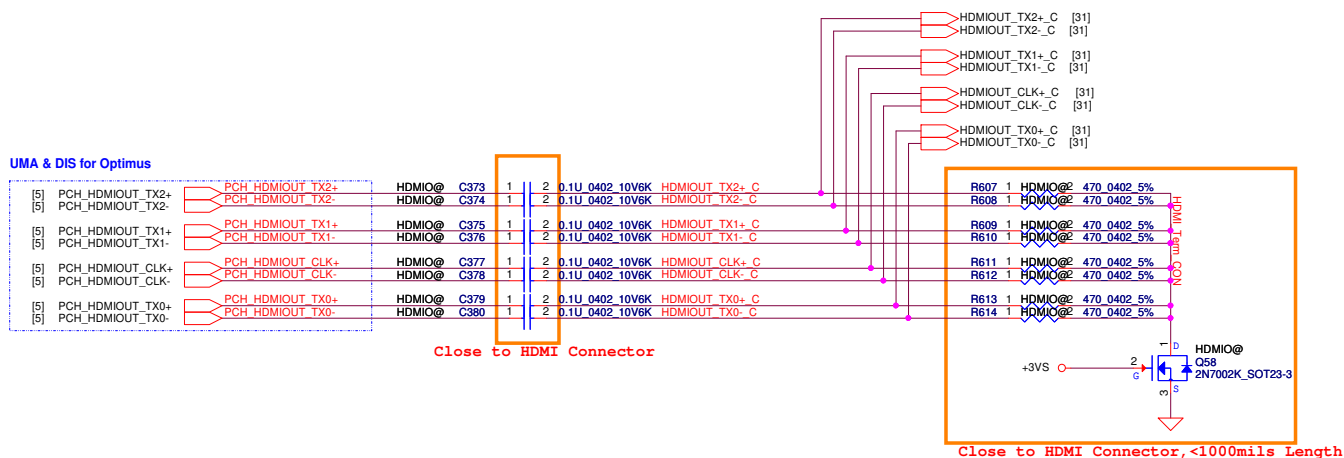
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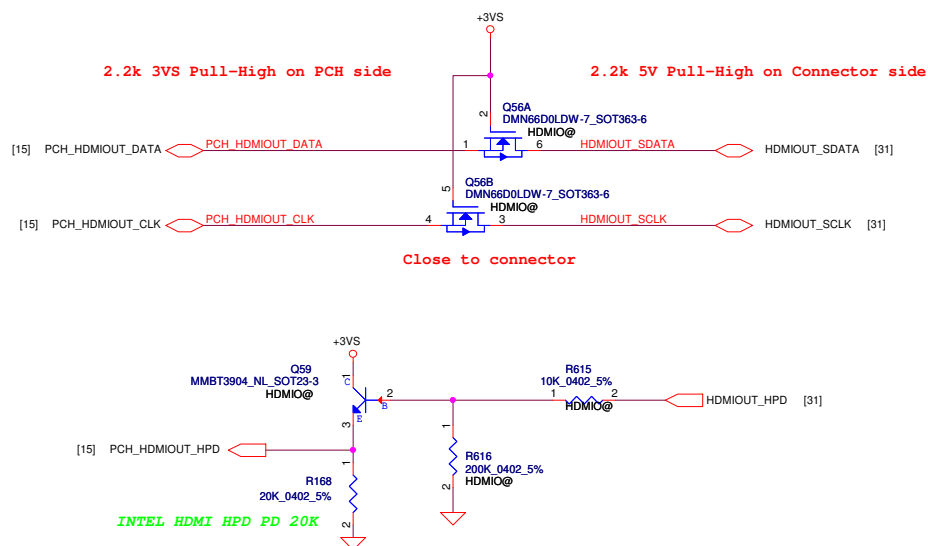
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UMA & DIS for Optimus

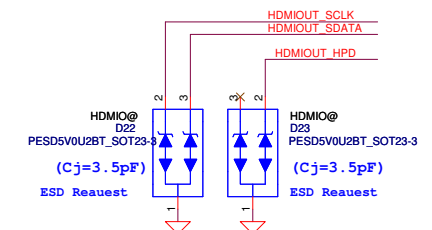
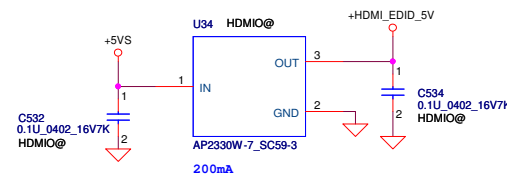
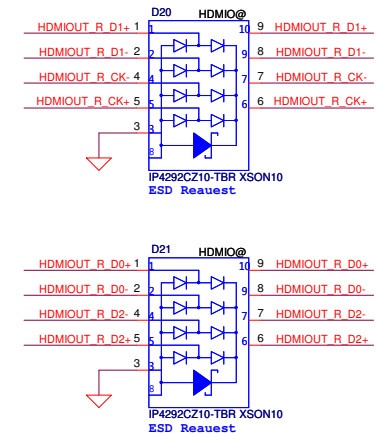
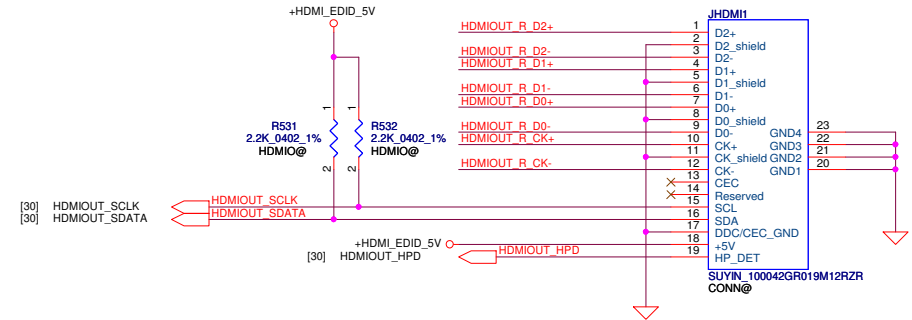
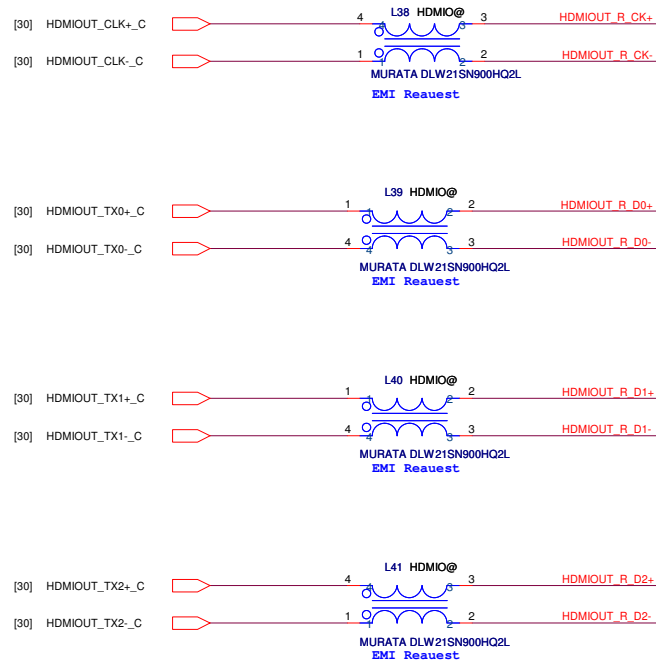


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| Size  | Custom                      | Document Number    | ZEA00 LA-A061P M/B |                          | Rev |
| Date:   | Tuesday, September 24, 2013 | Sheet              | 30                 | of                       | 59  |

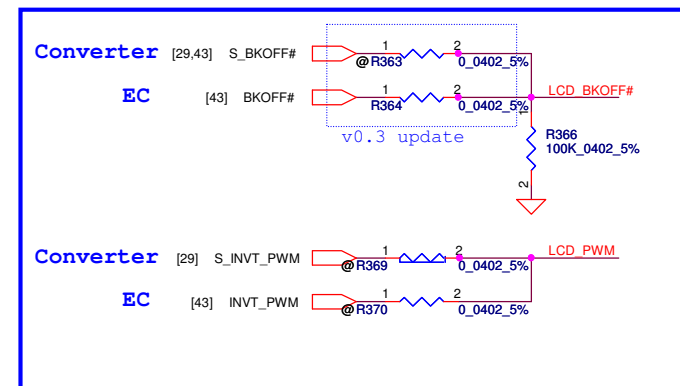
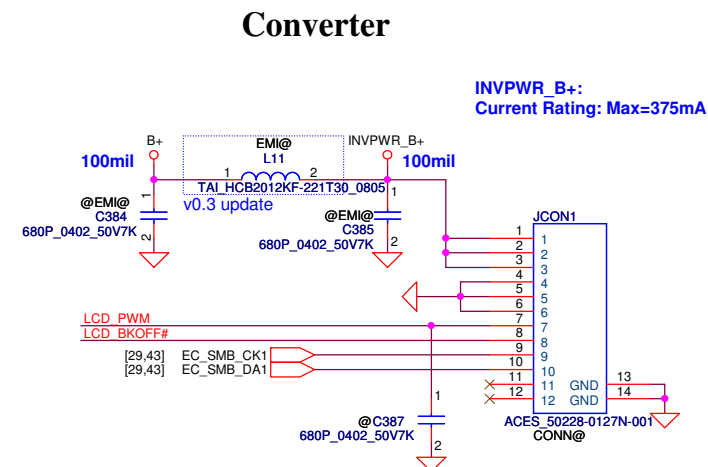
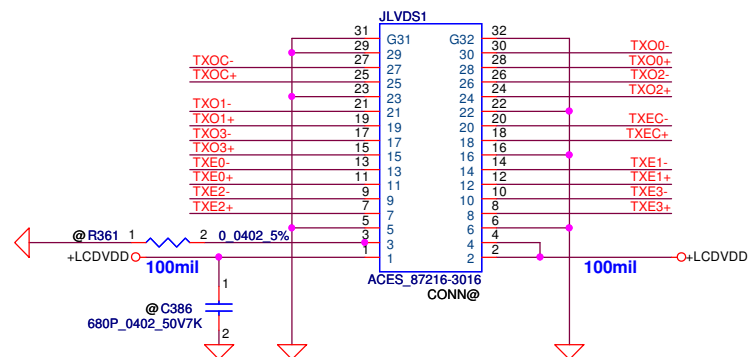
## HDMI-OUT Connector



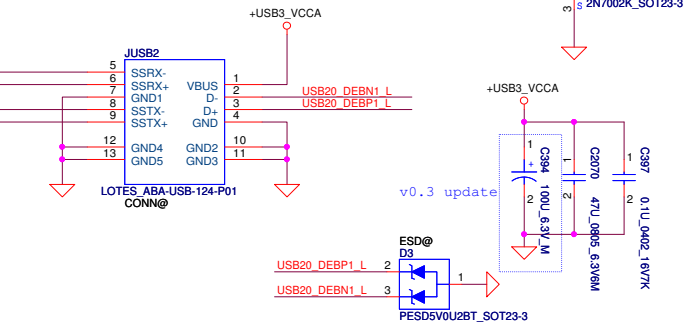
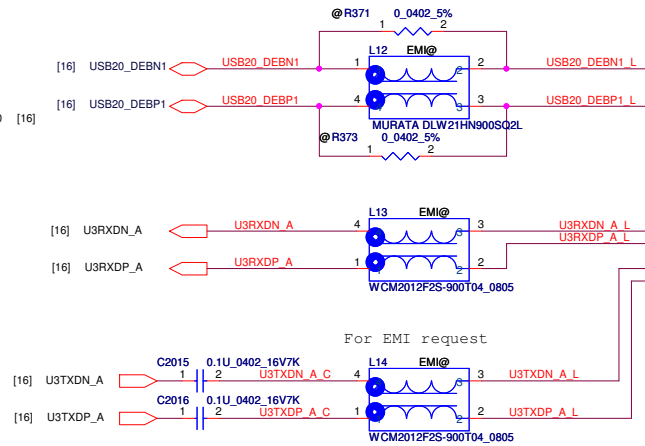
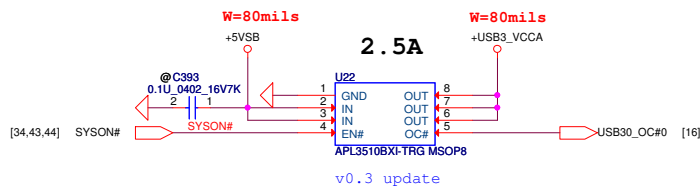
MURATA DLW21SN900HQ2L  
EMI Request

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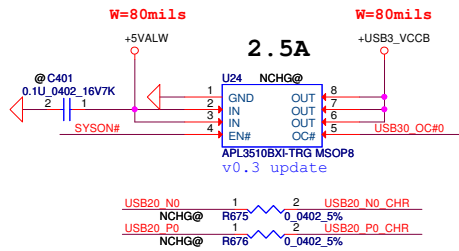
|   |            |                    |            |                                 |                             |            |          |
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| Security Classification   |            | Compal Secret Data |            | <b>Compal Electronics, Inc.</b> |                             |            |          |
| Issued Date   | 2013/04/01 | Deciphered Date    | 2014/04/01 | Title<br>HDMI-OUT               |                             |            |          |
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|   |            |                    |            | Custom                          | ZEA00 LA-A061P M/B          |            |          |
|   |            |                    |            | Date:                           | Tuesday, September 24, 2013 | Sheet      | 31 of 59 |



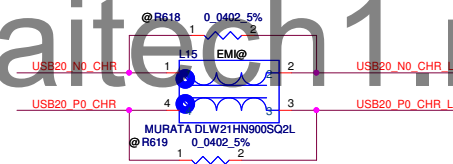
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| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc. |                 |         |
| Issued Date   | 2013/04/01         | Deciphered Date | 2014/04/01 | Title                    |                 |         |
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|   |                    |                 |            | Size B                   | Document Number | Rev 0.3 |
|   |                    |                 |            | ZEA00 LA-A061P M/B       |                 |         |
| Date: Tuesday, September 24, 2013   |                    |                 |            | Sheet                    | 32              | of 59   |



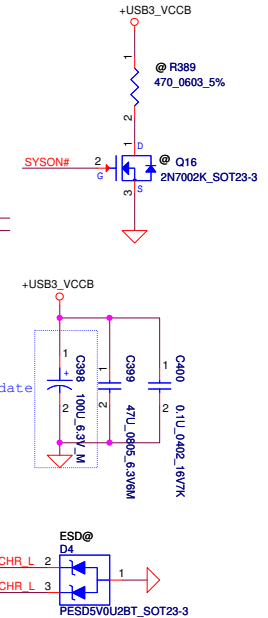
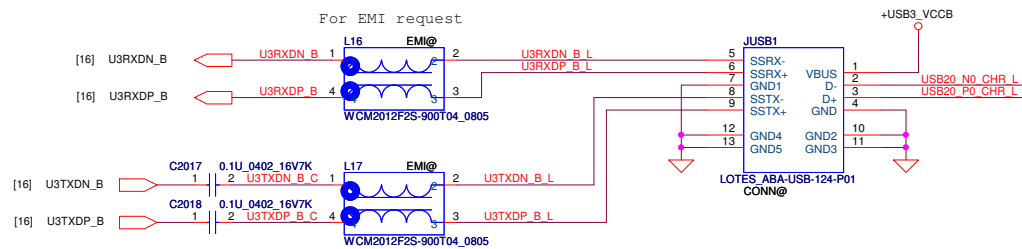
## Non Changer



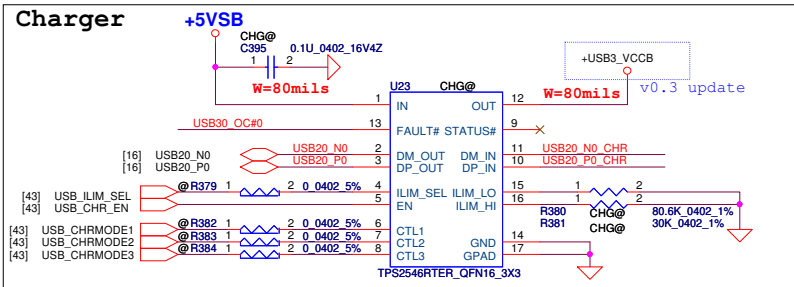
www.aitech1.ru



## Charge USB Port

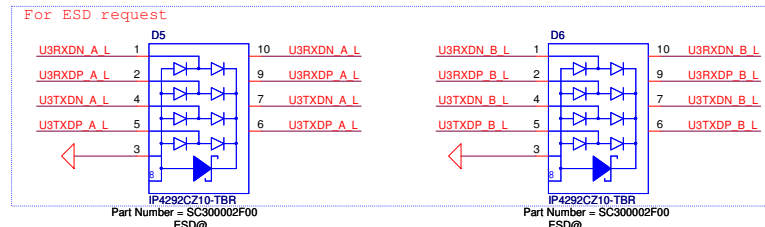


## Charger



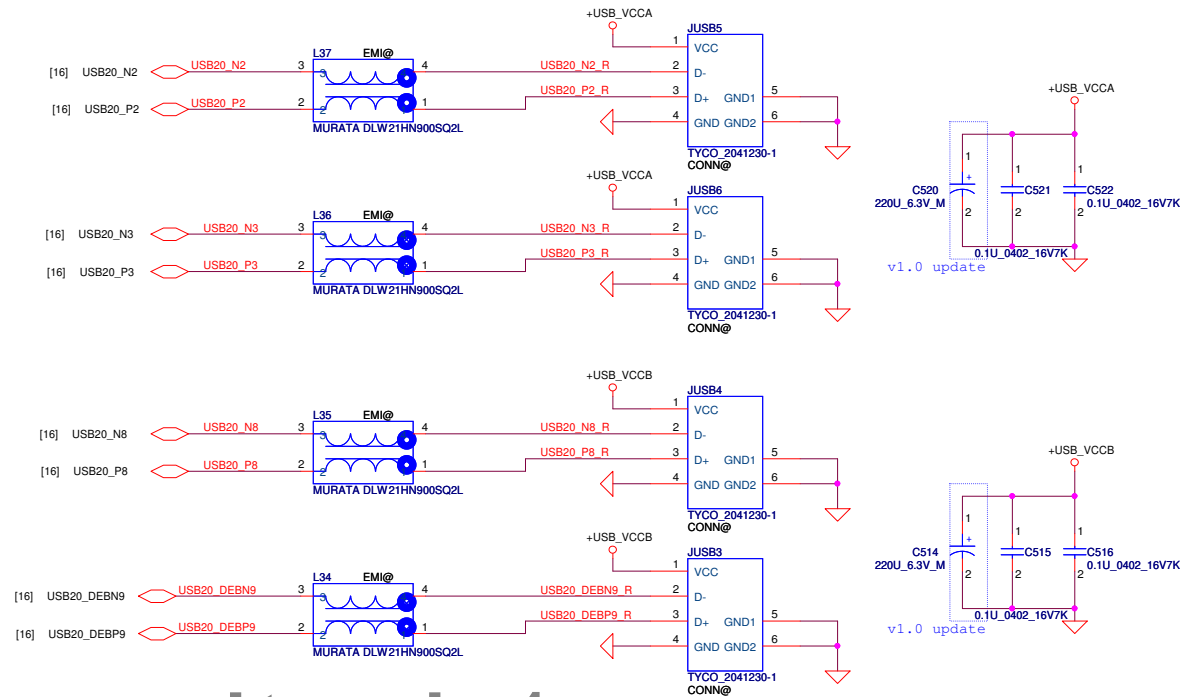
| Charger CT  | CTL1            | CTL2          | CTL3            | ILIM_SEL      |
|-------------|-----------------|---------------|-----------------|---------------|
| EC GPIO     | GPIOA07(pin104) | GPIO22(pin41) | GPIOA11(pin108) | GPIO21(pin40) |
| S0 (CDP)    | 1               | 1             | 1               | 1             |
| S3 (SDP)    | 1               | 1             | 1               | 1             |
| S4/S5 (DCP) | 0               | 0             | 1               | 1             |

| System Global Power State | TPS2546/TPS2544 Mode  | Charging | CTL1 | CTL2 | CTL3 | ILIM_SEL | Current Limit Setting |
|---------------------------|---|----------|------|------|------|----------|-----------------------|
| S3                        | SDP, no discharge to / from CDP   |          | 1    | 1    | 1    | 0        | ILIM_LO               |
| S0                        | CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs |          | 1    | 1    | 1    | 1        | ILIM_HI               |
| S4/S5                     | Auto mode, load detection with power wake thresholds, no mouse wake                       |          | 0    | 0    | 1    | 1        | ILIM_HI               |



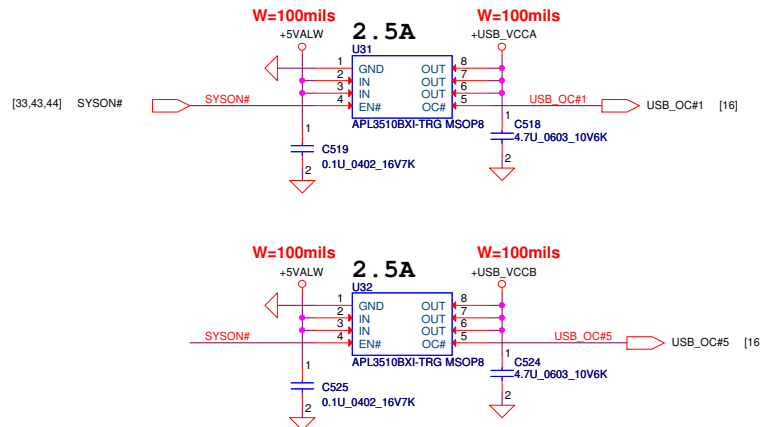
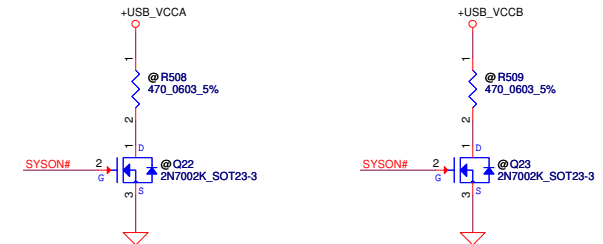
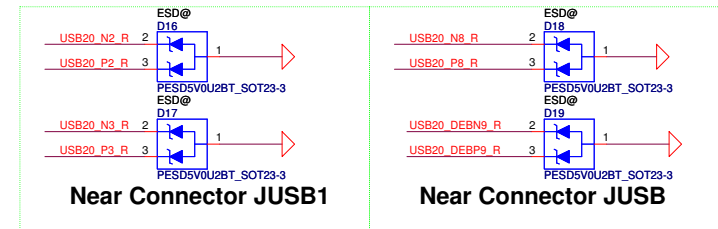
| Security Classification   | Compal Secret Data | Title              |
|---|--------------------|--------------------|
| Issued Date   | Deciphered Date    | USB 3.0 CONN       |
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| Part Number = SC300002F00   |                    | Document Number    |
| ESD@  |                    | ZEA00 LA-A061P M/B |
| Part Number = SC300002F00   |                    | Rev 0.3            |
| ESD@  |                    | Sheet 33 of 59     |

# USB20



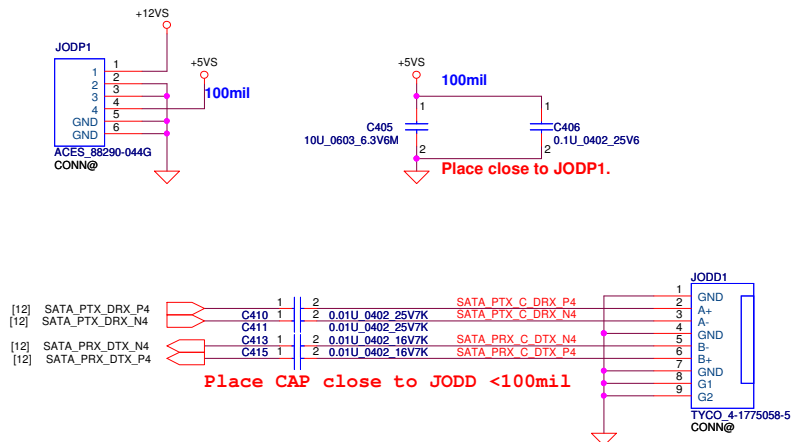
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For USB2.0 ESD diode

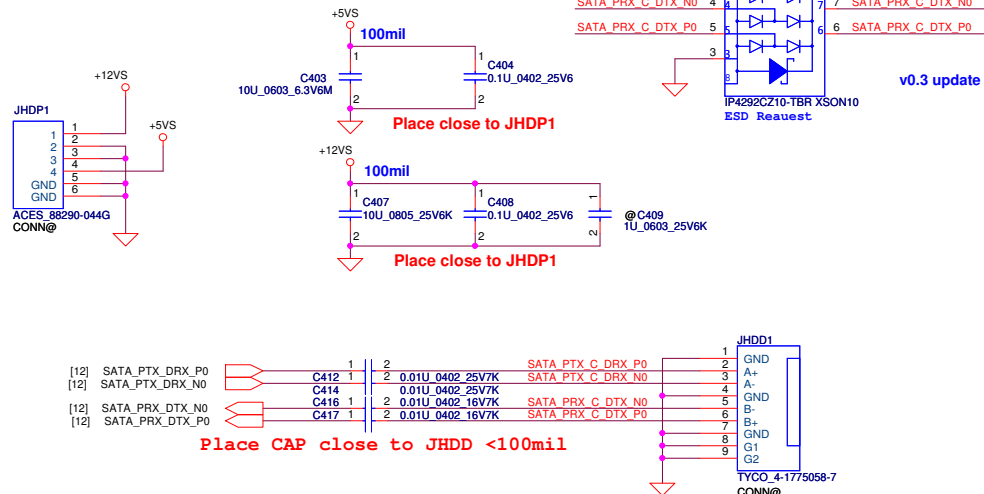


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| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc. |                             |
| Issued Date   | 2013/04/01         | Deciphered Date | 2014/04/01 | Title                    | USB20                       |
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|   |                    |                 |            |                          | Document Number             |
|   |                    |                 |            |                          | ZEAO0 LA-A061P M/B          |
|   |                    |                 |            |                          | Rev                         |
|   |                    |                 |            |                          | 0.3                         |
|   |                    |                 |            |                          | Date                        |
|   |                    |                 |            |                          | Tuesday, September 24, 2013 |
|   |                    |                 |            |                          | Sheet                       |
|   |                    |                 |            |                          | 34 of 59                    |

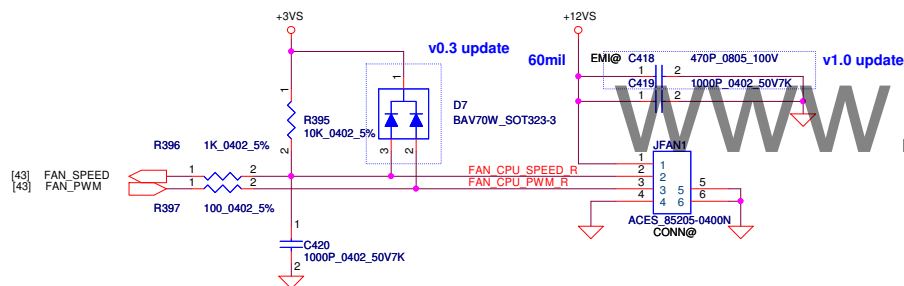
## SATA ODD Conn



## SATA HDD Conn.

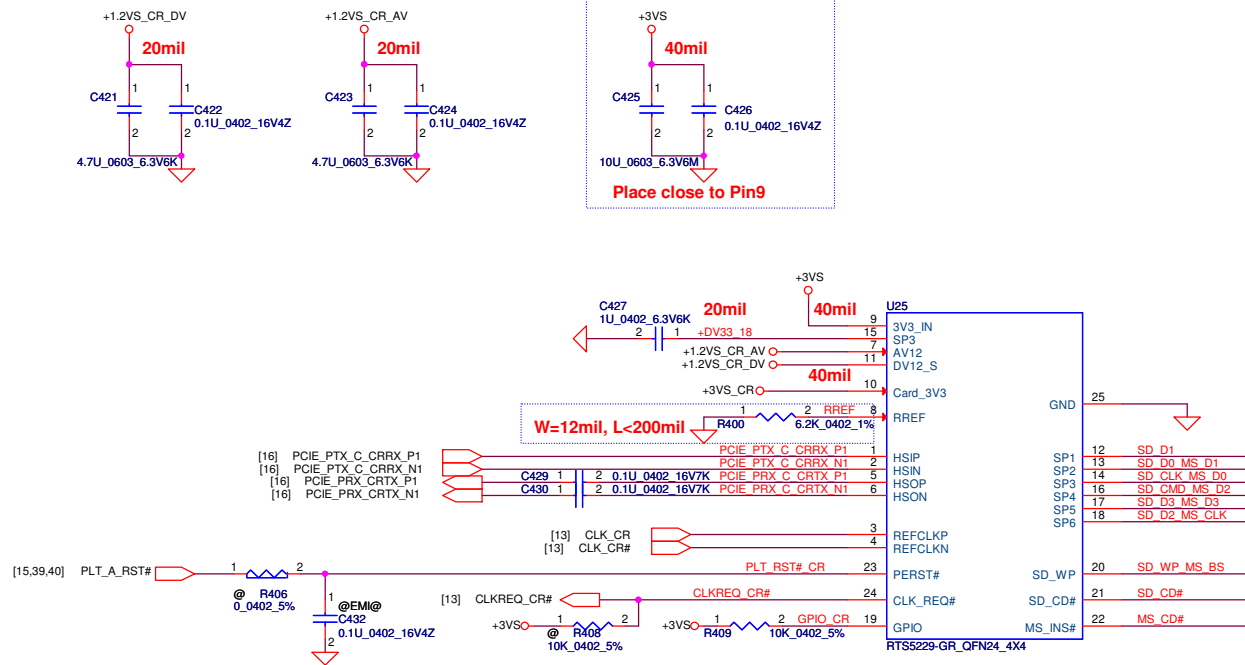


## FAN Control Circuit

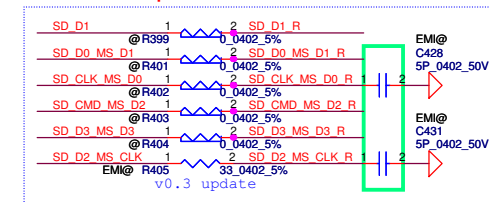


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| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |                             |
| Issued Date   | 2013/04/01 | Deciphered Date    | 2014/04/01 | Title                    | SATA-HDD/ODD/USB            |
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|   |            |                    |            |                          | ZEA00 LA-A061P M/B          |
|   |            |                    |            | Date                     | Tuesday, September 24, 2013 |
|   |            |                    |            | Sheet                    | 35 of 59                    |
|   |            |                    |            | Rev                      | 0.3                         |

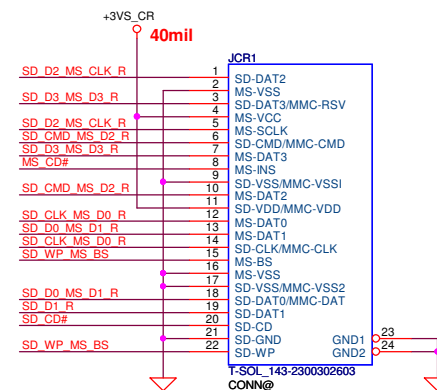
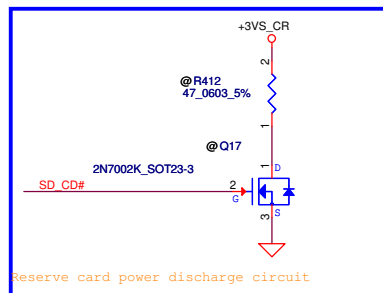
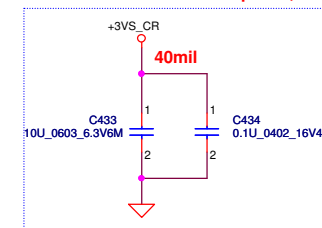
www.aitech1.ru



Length of per trace 2inch no more 2 via  
mismatch trace length <100mil  
50ohm +-15% impedance.



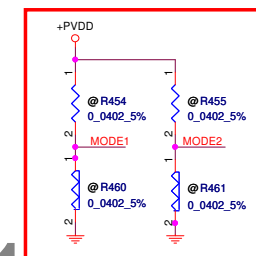
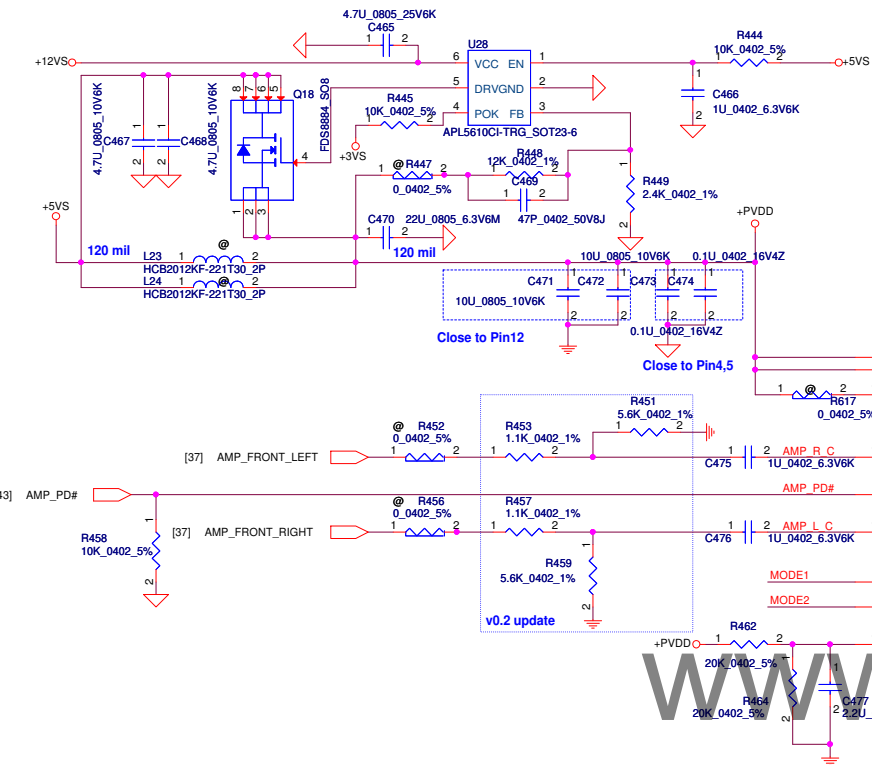
Place close to JCR1 pin 12,21



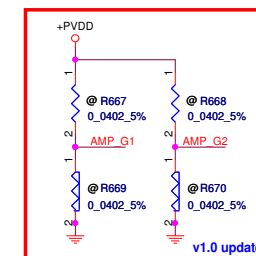
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| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |                             |
| Issued Date   | 2013/04/01 | Deciphered Date    | 2014/04/01 | Title                    |                             |
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|   |            |                    |            | Custom                   | 0.3                         |
|   |            |                    |            | Document Number          |                             |
|   |            |                    |            | ZEA00 LA-A061P M/B       |                             |
|   |            |                    |            | Date:                    | Tuesday, September 24, 2013 |
|   |            |                    |            | Sheet                    | 36 of 59                    |







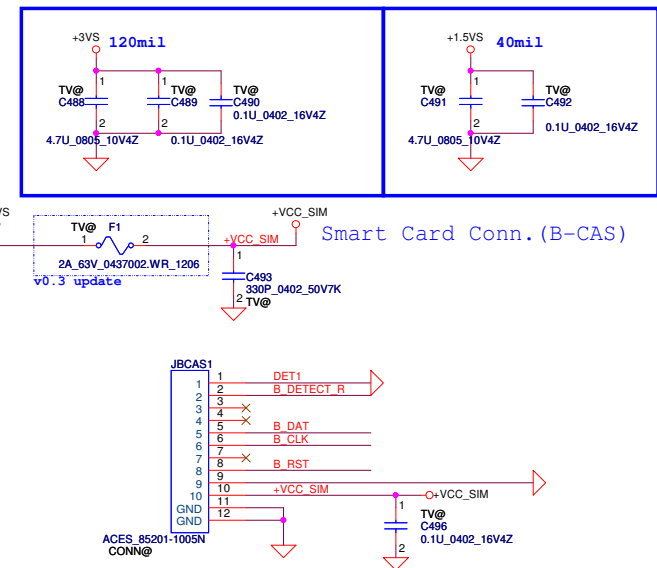
| Model | Mode2 | Option     | Pin15 | Pin16 |
|-------|-------|------------|-------|-------|
| 0     | 0     | Fixed Gain | G1    | G2    |
| 0     | 1     | I2C        | SCL   | SDA   |
| 1     | 0     | PWM        | PWM   | Hold  |
| 1     | 1     | DC         | DC    | Hold  |



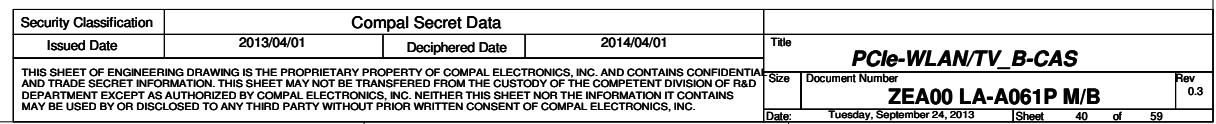
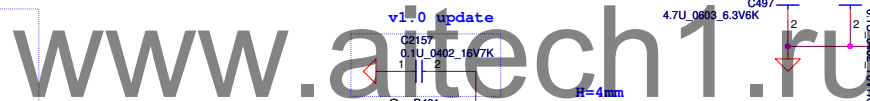
| AMP_G1 | AMP_G2 | Gain |
|--------|--------|------|
| 0      | 0      | 11dB |
| 0      | 1      | 14dB |
| 1      | 0      | 19dB |
| 1      | 1      | 25dB |



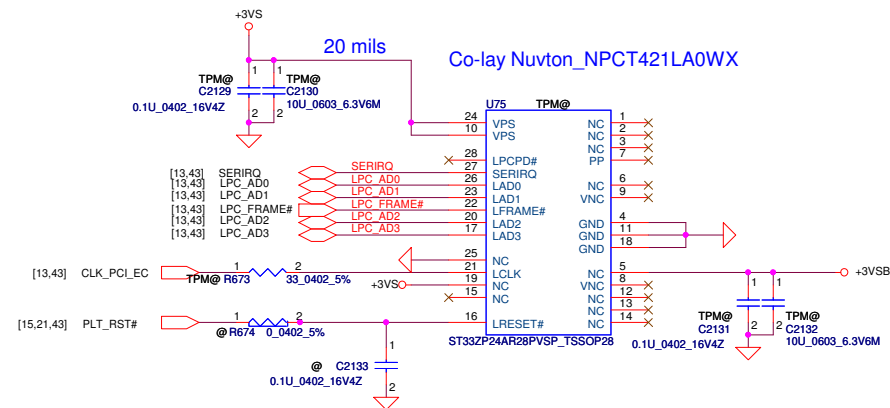
Mini Card Slot 1---TV tuner Current: +3VS : 2750mA, 1.5V: 500mA



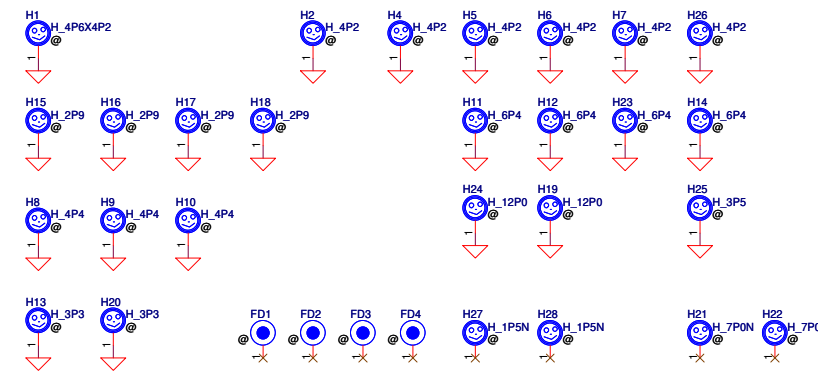
**Mini Card Slot 2--- WLAN Current: 3.3 : 750mA,**



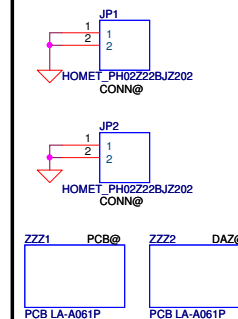
## TPM (Reserve)



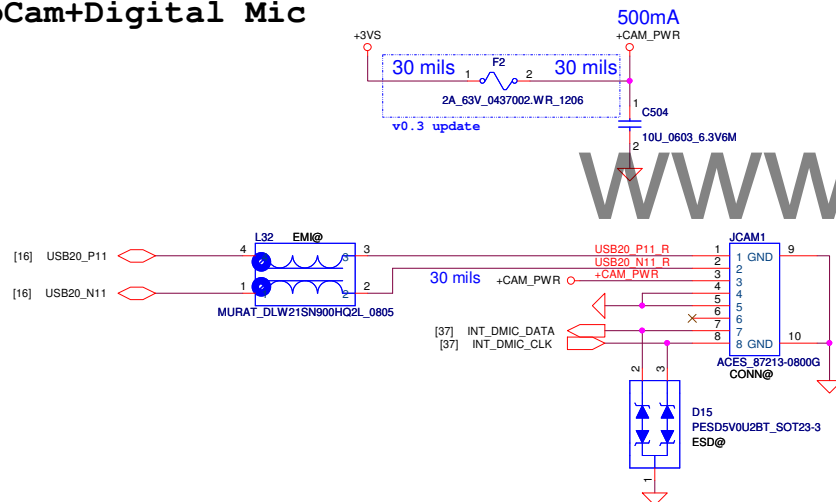
## Screw Hole



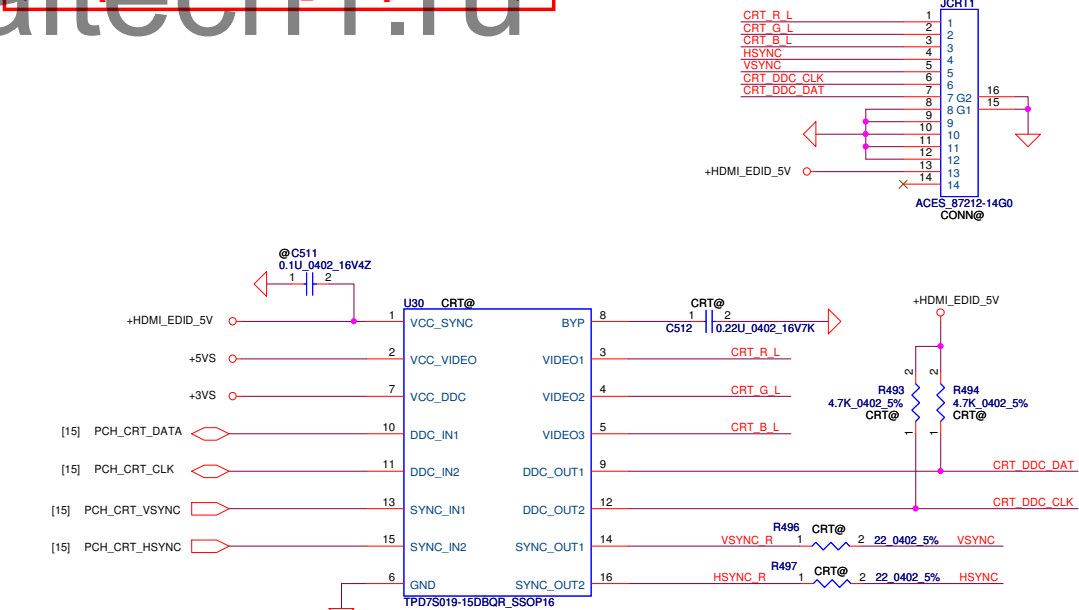
## PCH heat sink



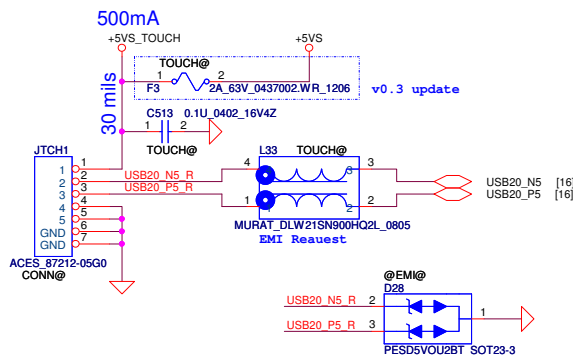
## WebCam+Digital Mic



Need PU/PL on PCH/PCH side  
(2.2K\*2pcs for DDC & 150\_8P4R\*1pcs for RGB)



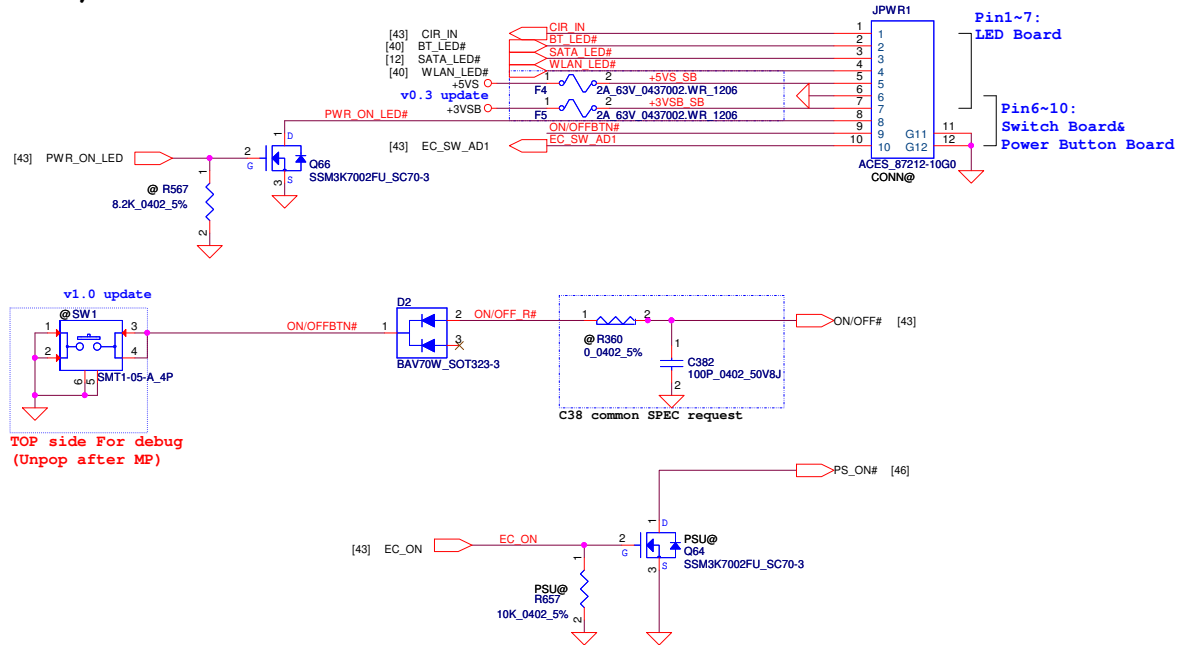
## Touch



| Security Classification   |            | Compal Secret Data |            | Title                       |                 |
|---|------------|--------------------|------------|-----------------------------|-----------------|
| Issued Date   | 2013/04/01 | Deciphered Date    | 2014/04/01 | Size                        | Document Number |
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|   |            |                    |            | ZEA00 LA-A061P M/B          |                 |
|   |            |                    |            | Date:                       | Rev             |
|   |            |                    |            | Tuesday, September 24, 2013 | 0.3             |
|   |            |                    |            | Sheet                       | 41 of 59        |

Power/B & SW/B Connector

8Pin sub-board Connecetor

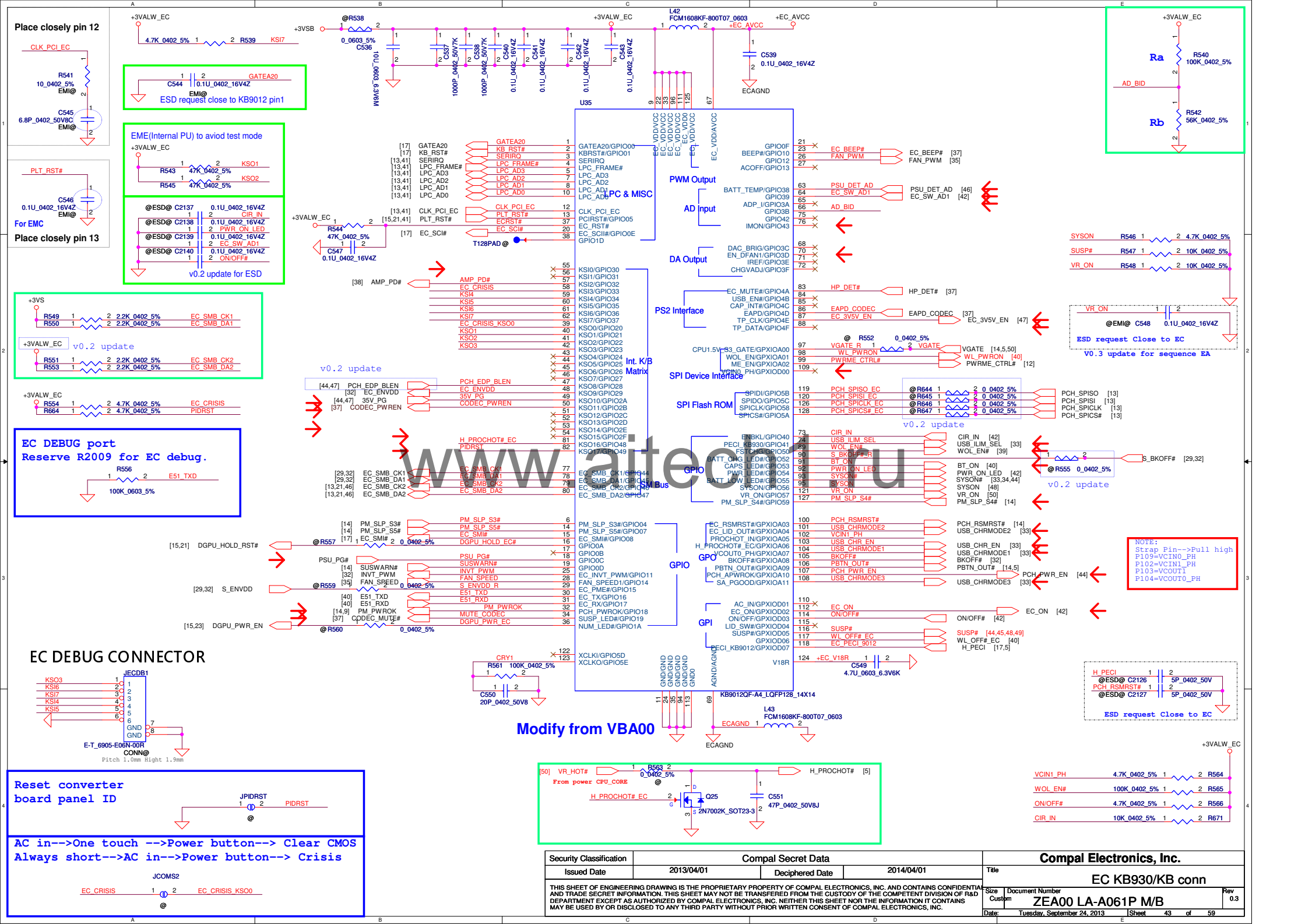


TOP side For debug  
(Unpop after MP)

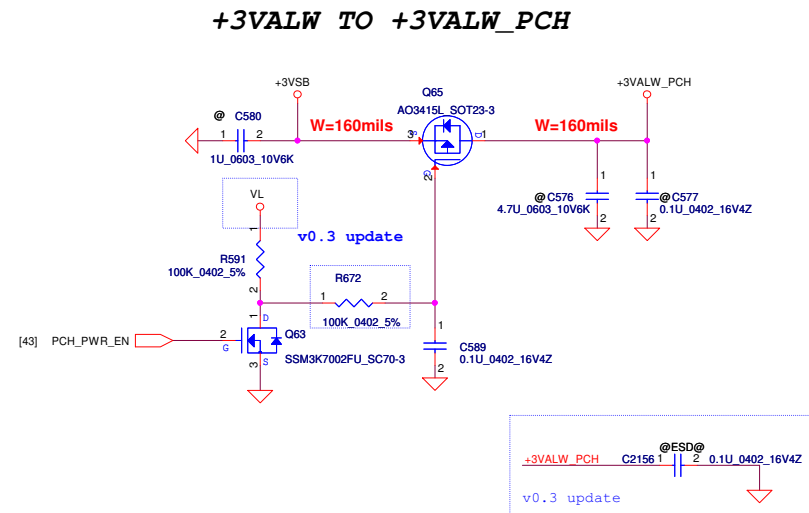
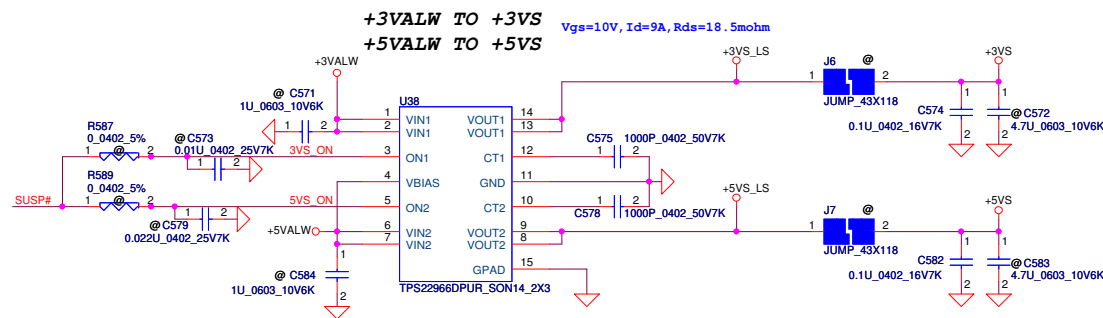
|             |            |   |   |                 |
|-------------|------------|---|---|-----------------|
| +5VS_SB     | EMI@ C2144 | 1 | 2 | 0.1U_0402_16V4Z |
| +3VSB_SB    | EMI@ C2145 | 1 | 2 | 470P_0402_50V7K |
| CIR_IN      | EMI@ C2146 | 1 | 2 | 330P_0402_50V7K |
| BT_LED#     | EMI@ C2147 | 1 | 2 | 330P_0402_50V7K |
| SATA_LED#   | EMI@ C2148 | 1 | 2 | 330P_0402_50V7K |
| WLAN_LED#   | EMI@ C2149 | 1 | 2 | 470P_0402_50V7K |
| PWR_ON_LED# | EMI@ C2150 | 1 | 2 | 470P_0402_50V7K |
| ON/OFFBTN#  | EMI@ C2151 | 1 | 2 | 470P_0402_50V7K |
| EC_SW_AD1   | EMI@ C2152 | 1 | 2 | 470P_0402_50V7K |

v1.0 update

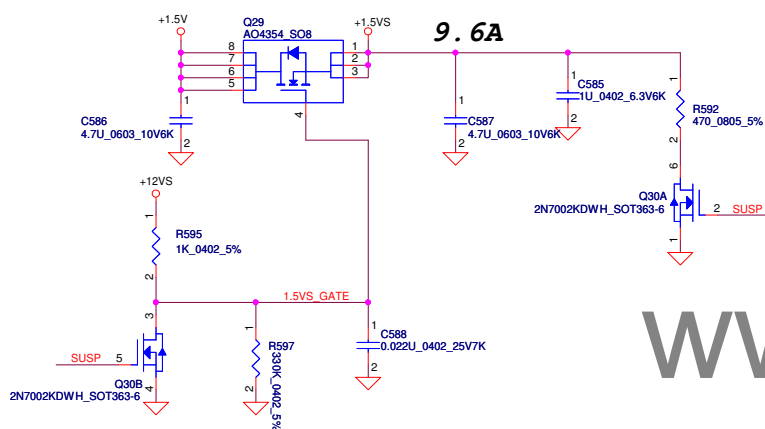
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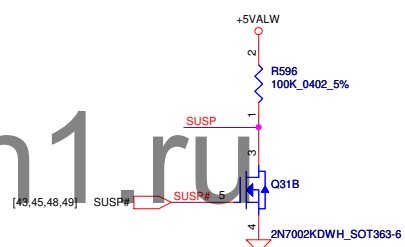




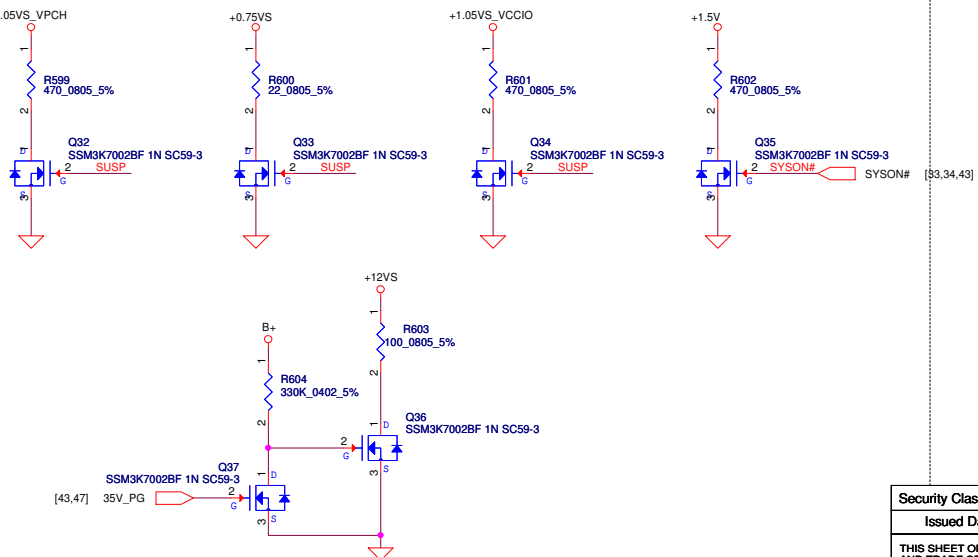
# +1.5V to +1.5VS



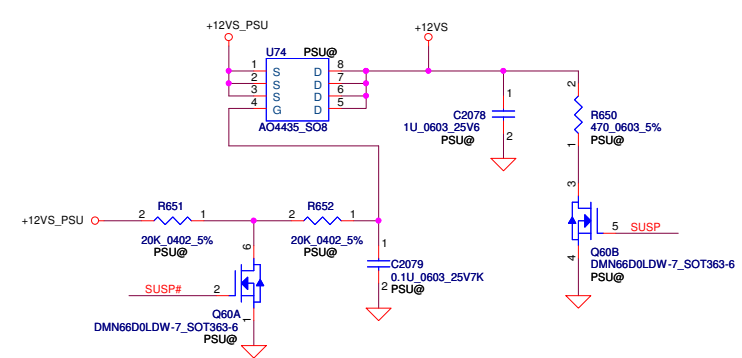
www.aitech1.ru



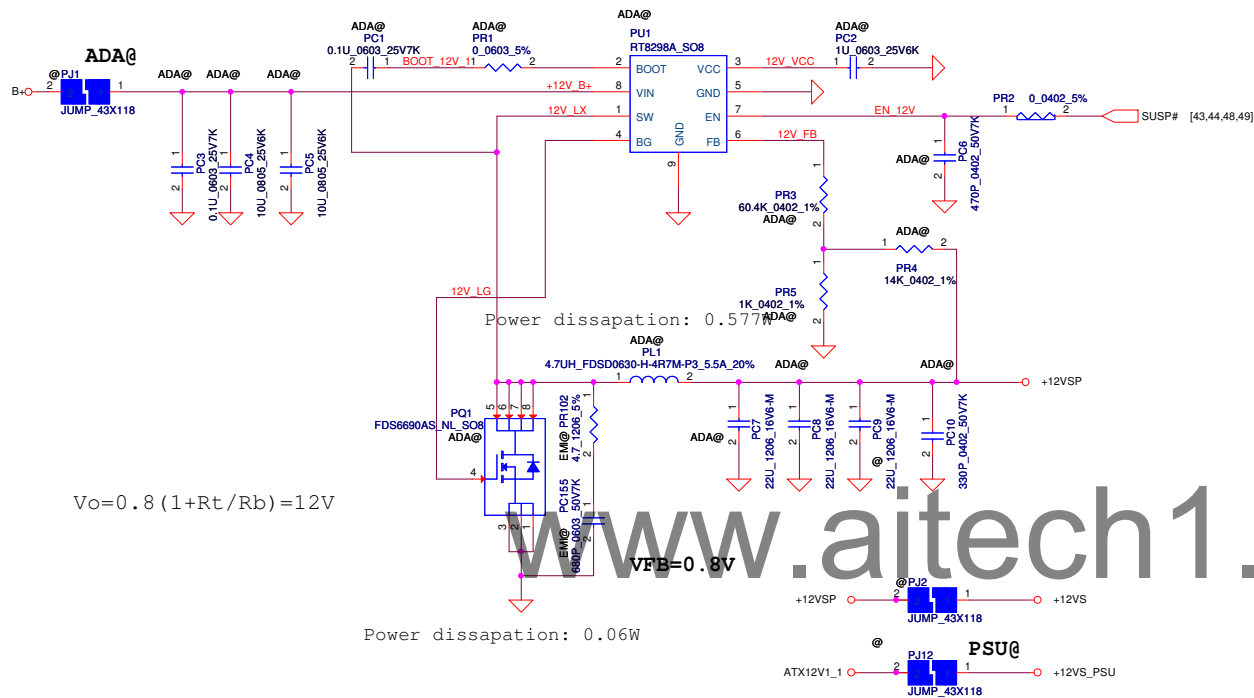
# Discharge circuit



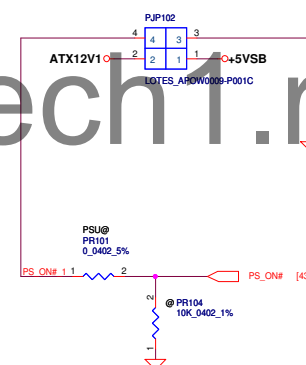
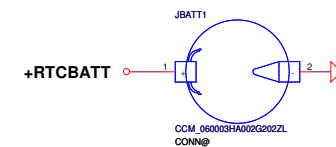
# +12V1 TO +12VS (Reserve for PSU)



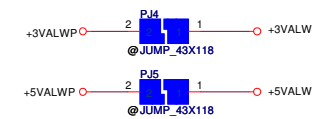
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| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |                             |
| Issued Date   | 2013/04/01 | Deciphered Date    | 2014/04/01 | Title                    |                             |
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|   |            |                    |            | Size                     | Document Number             |
|   |            |                    |            |                          | ZEA00 LA-A061P M/B          |
|   |            |                    |            | Rev                      | 0.3                         |
|   |            |                    |            | Date                     | Tuesday, September 24, 2013 |
|   |            |                    |            | Sheet                    | 44 of 59                    |



|   |            |                    |            |                   |          |
|---|------------|--------------------|------------|-------------------|----------|
| Security Classification   |            | Compal Secret Data |            | Title             |          |
| Issued Date   | 2012/04/27 | Deciphered Date    | 2013/04/27 | PWR- 12VSP        |          |
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|   |            |                    |            | VBA11 LA-A111 M/B | 0.1      |
| Date: Tuesday, September 24, 2013   |            |                    |            | Sheet             | 45 of 56 |



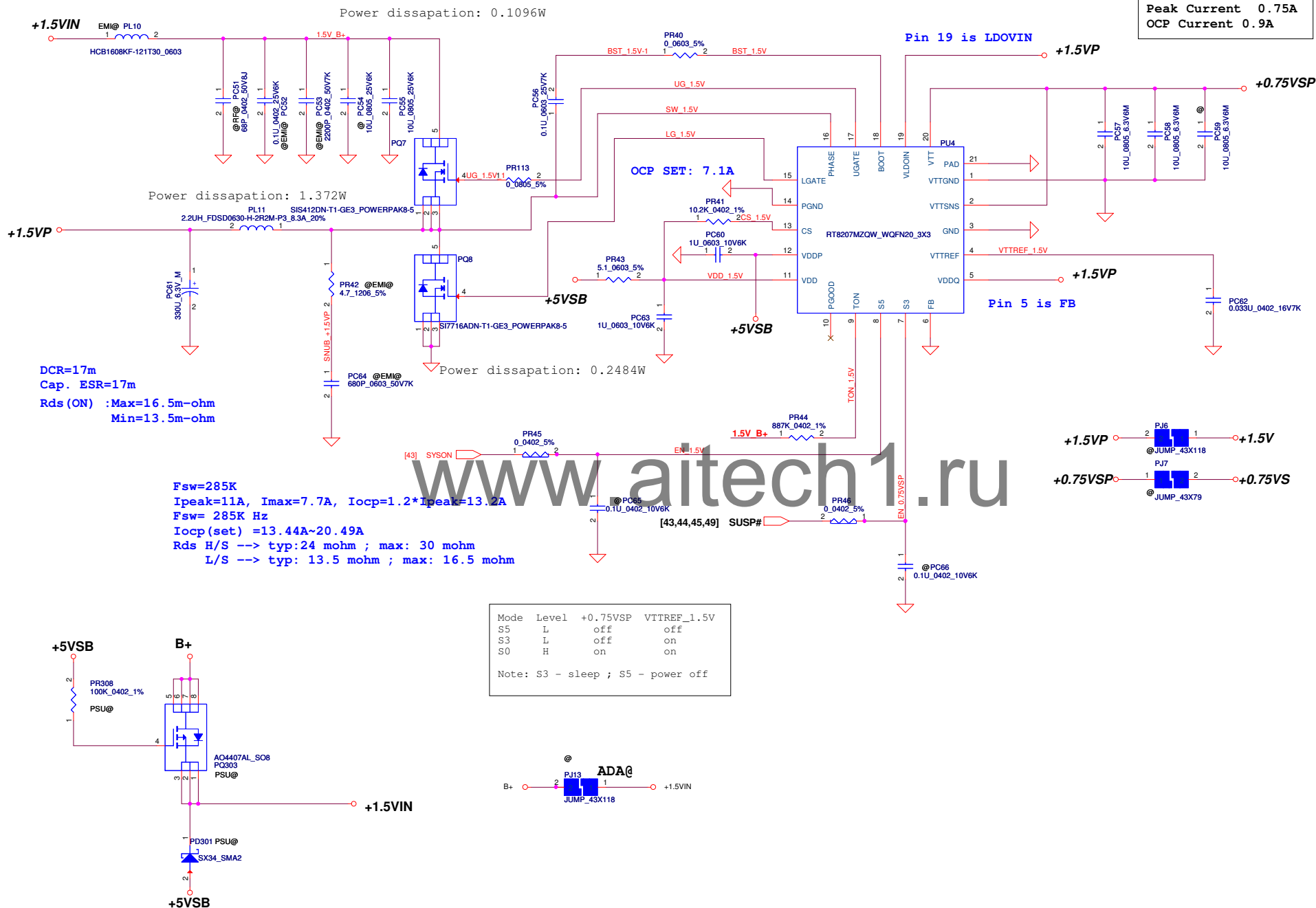
```
Ventura for CPU side
slave address : 1000001
please placemnet near R-sense
```



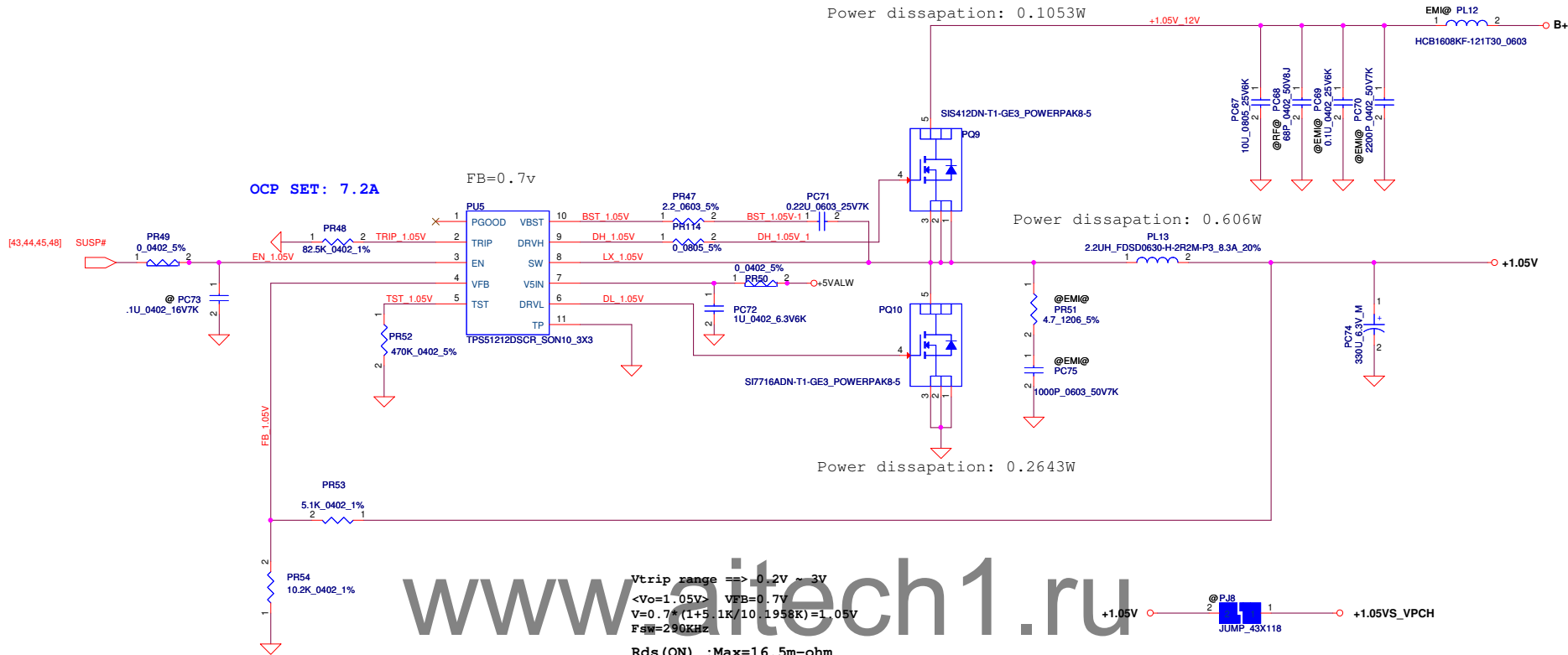
TON (1) SMPS1=300KHZ (+5VALWP)  
(2) SMPS2=300KHZ (+3VALWP)

Rev  
0.1

|   |            |                    |            |  |                    |
|---|------------|--------------------|------------|--|--------------------|
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|   |            |                    |            | Document Number  | VCA00 LA-9792P M/B |
|   |            |                    |            | Tuesday, September 24, 2013                                  | Sheet 47 of 56     |



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|   |                    |                 |            | 1.5VP                             | 0.1            |
|   |                    |                 |            | Date: Tuesday, September 24, 2013 | Sheet 48 of 56 |

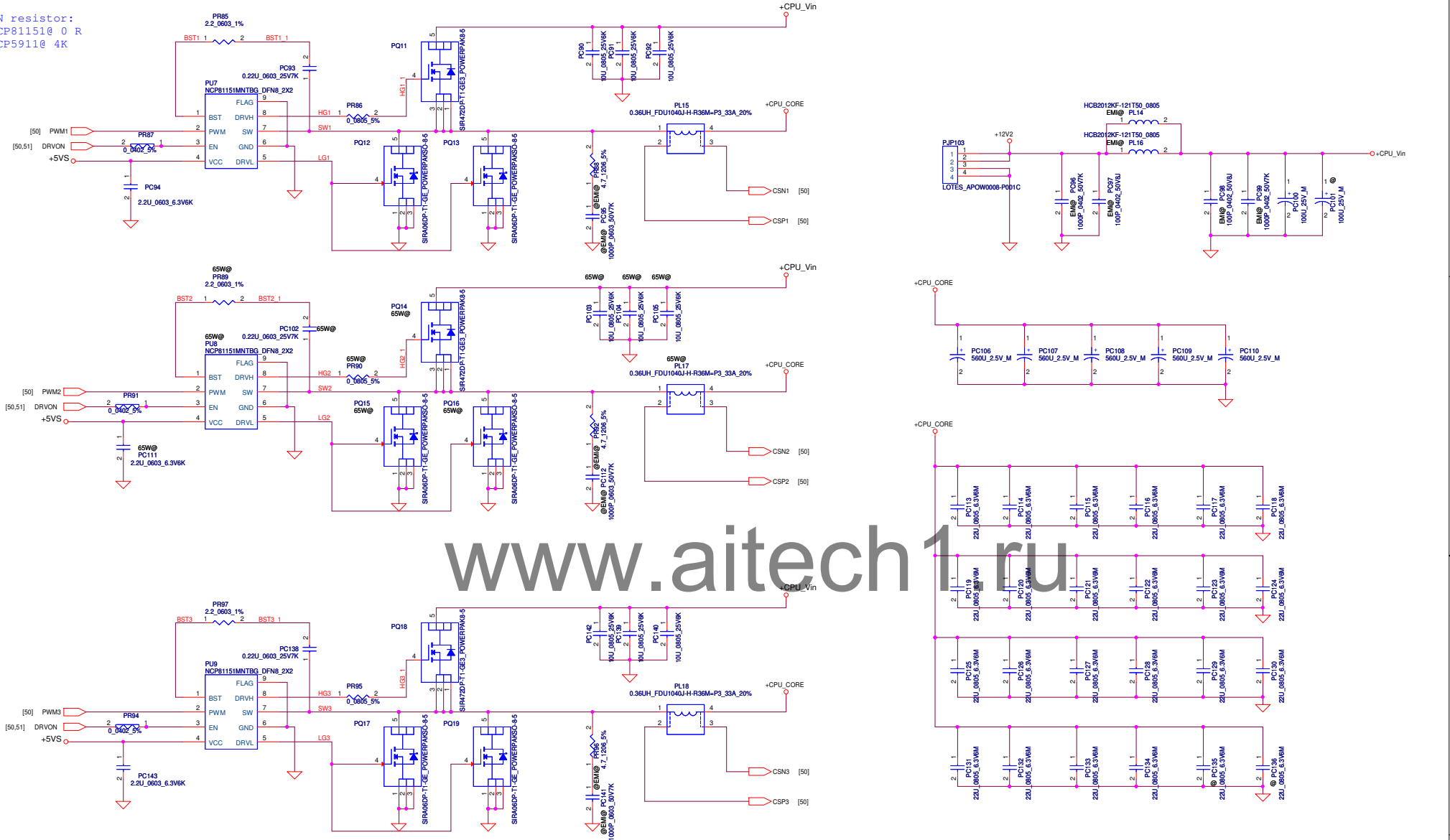


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|   |            |                    |            | Date                     | Tuesday, September 24, 2013 |
|   |            |                    |            | Sheet                    | 49 of 56                    |





EN resistor:  
NCP81151@ 0 R  
NCP5911@ 4K

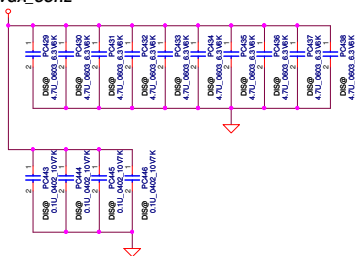


|             |                             |                |
|-------------|-----------------------------|----------------|
| Title       |                             |                |
| Power Stage |                             |                |
| Size        | Document Number             | Rev            |
|             | VCA00 LA-9792P M/B          | 0.1            |
| Date:       | Tuesday, September 24, 2013 | Sheet 51 of 56 |

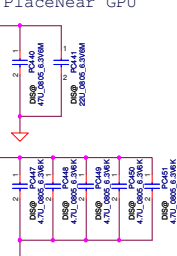
Design for  
N14M-GE2

Follow GB4-128 demand

+VGA\_CORE Place Under GPU



+VGA\_CORE PlaceNear GPU

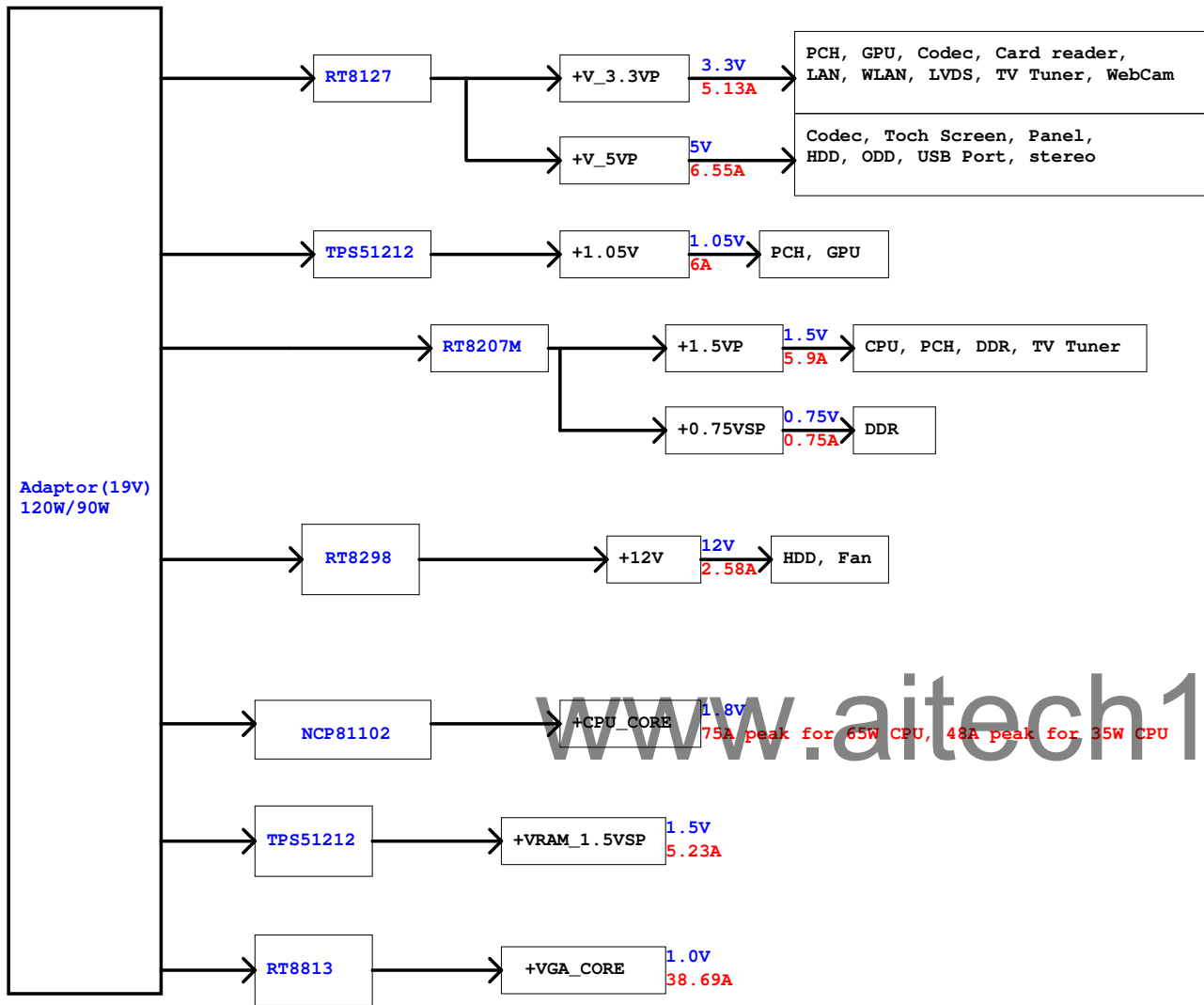


PH701 close to MOSFET  
Trigger point 110 degree

N14P-GE2  
Ipeak=  
Imax=  
Iocp=

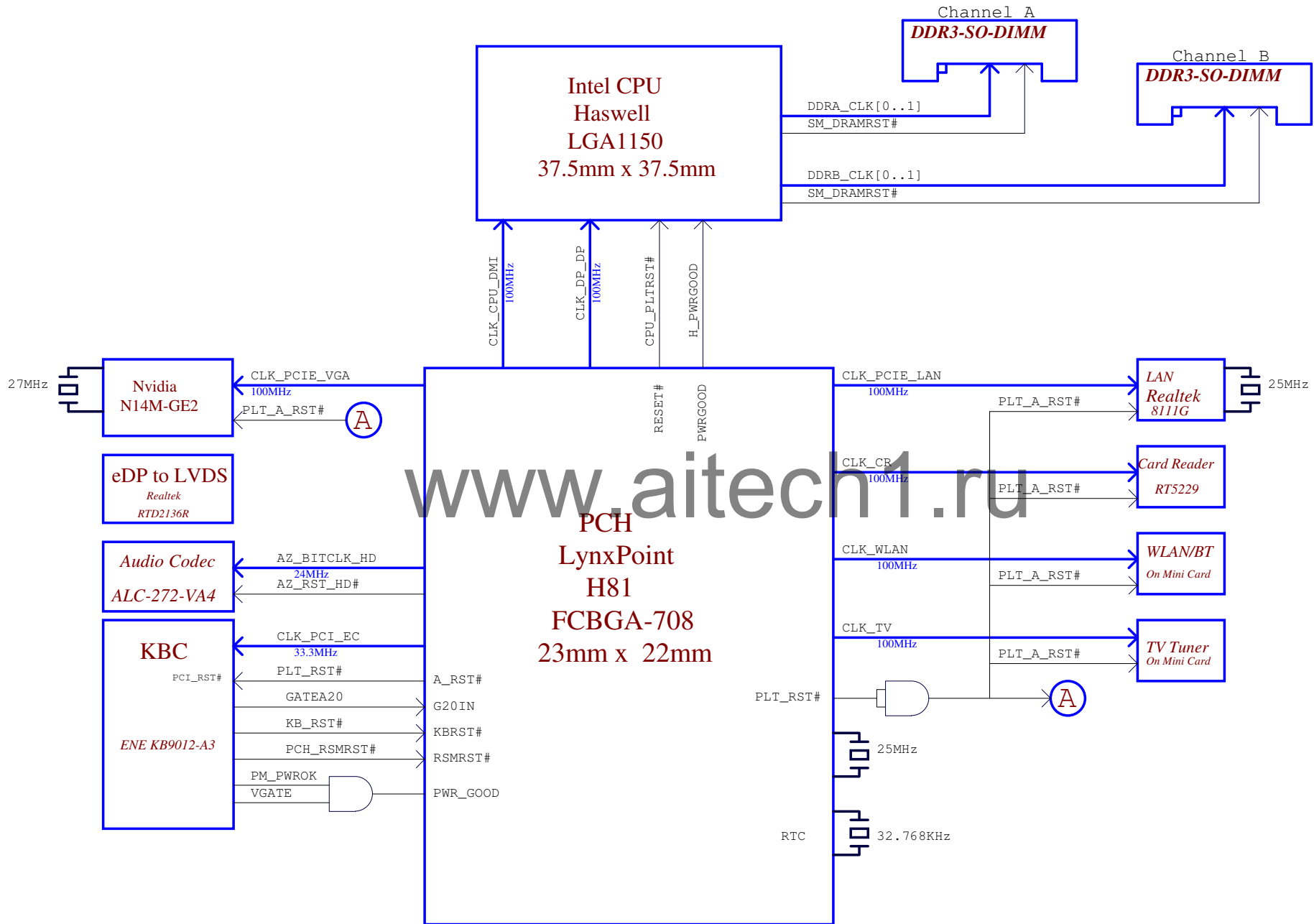
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|---|------------|--------------------|------------|--------------------------|-----------------------|
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|   |            |                    |            | Date                     | Tripoli               |
|   |            |                    |            | Version                  | September 24, 2013    |
|   |            |                    |            | Sheet                    | 52 of 56              |
|   |            |                    |            | Rev                      | 0.1                   |



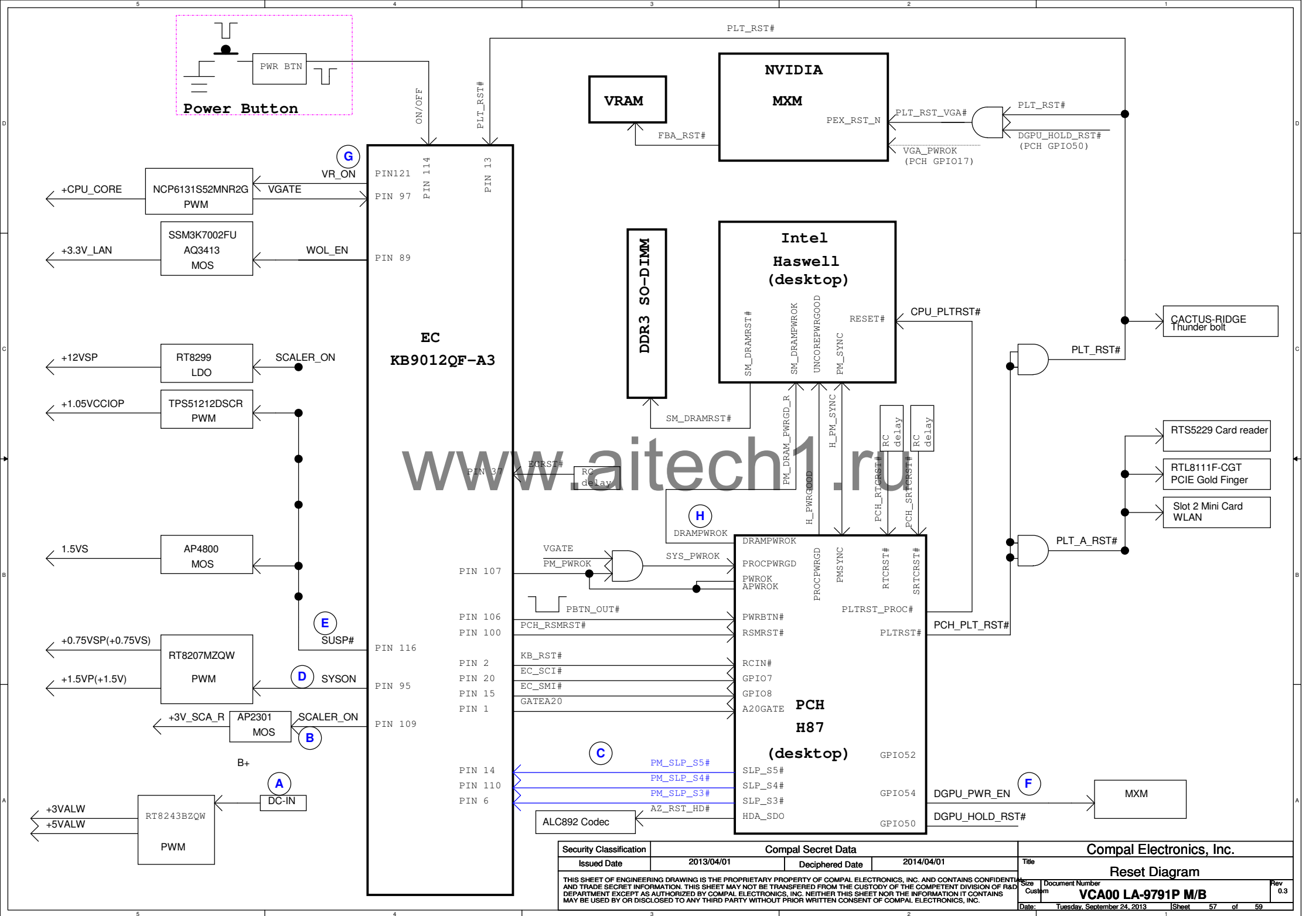


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|---|------------|--------------------|------------|-----------------------------------|----------|
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|   |            |                    |            | Custom                            | 0.4      |
|   |            |                    |            | Date: Tuesday, September 24, 2013 |          |
|   |            |                    |            | Sheet                             | 55 of 59 |

# Clock and Reset Diagram



|  |                    |                 |                          |       |
|--|--------------------|-----------------|--------------------------|-------|
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| Date: Tuesday, September 24, 2013  |                    |                 |                          | 0.3   |
| Sheet 56 of 59   |                    |                 |                          |       |



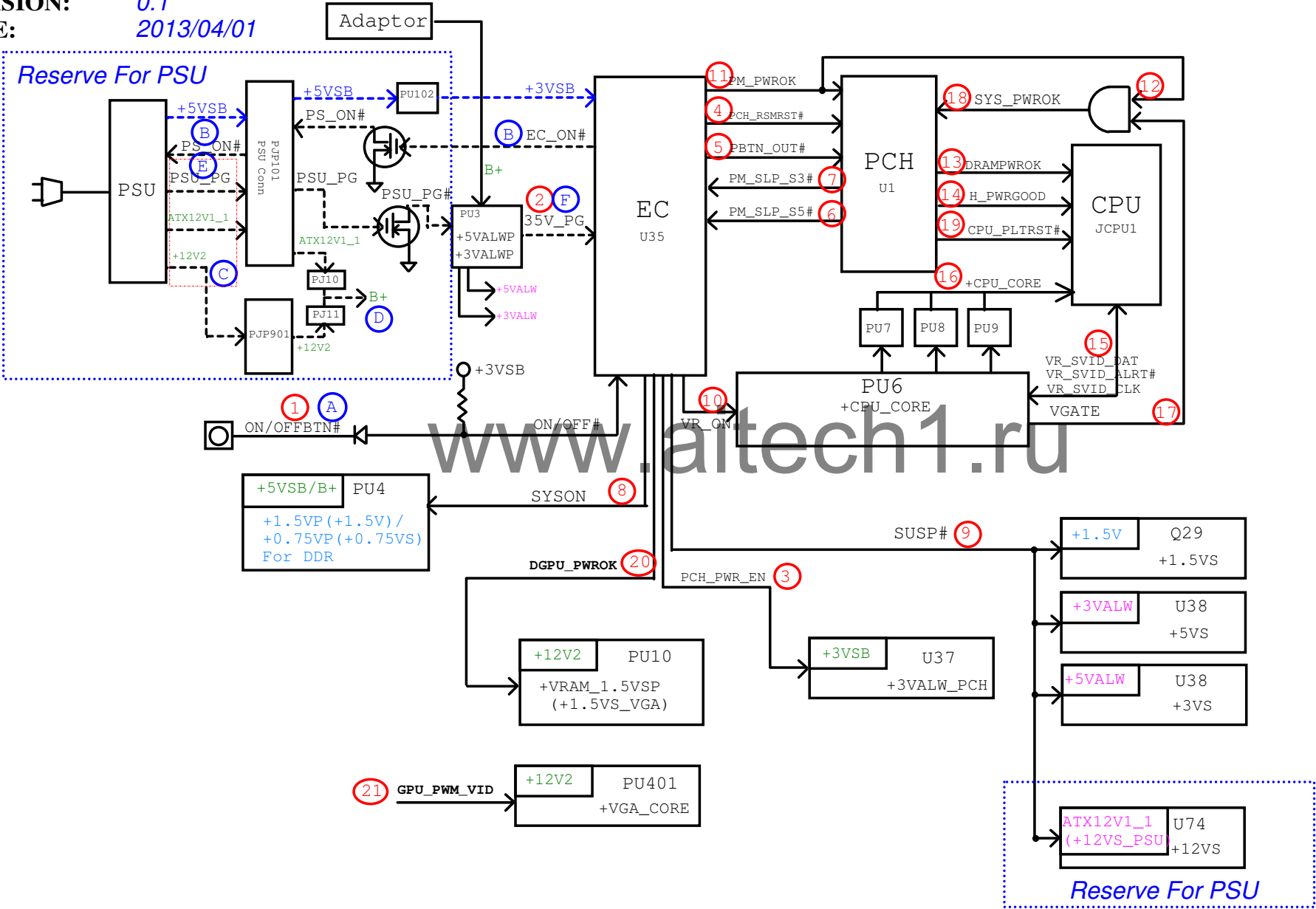
| NO |          | DATE | PAGE | MODIFICATION LIST                             | PURPOSE                 |
|----|----------|------|------|---|-------------------------|
| 1. | 20130604 | P47  |      | Add PC154 and Change the pu101 to SA00005A800 | For Pericom issue       |
| 2. | 20130729 | P45  |      | Add PR105 ,PC155 Shaber                       | For ENI Request         |
| 3. | 20130729 | P45  |      | Add PR1                                       | For ENI Request         |
| 3. | 20130729 | P45  |      | Add PR39                                      | For S5 power loss issue |

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MODEL NAME: ZEA00 Power Sequence Block Diagram (Discrete)  
PCB NAME: LA-A061P  
REVISION: 0.1  
DATE: 2013/04/01



|   |            |                    |            |                          |                             |
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| Issued Date   | 2013/04/01 | Deciphered Date    | 2014/04/01 | Title                    | Power Sequence Diagram      |
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|   |            |                    |            | Date                     | Tuesday, September 24, 2013 |
|   |            |                    |            | Sheet                    | 58 of 59                    |
|   |            |                    |            | Rev                      | 0.3                         |

HW PIR (Product Improve Record)

ZEA00 LA-A061P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 --> 0.2

GERBER-OUT DATE: 2013/06/20

| NO    | DATE | PAGE | MODIFICATION LIST  | PURPOSE |
|-------|------|------|--|---------|
| ----- |      |      |  |         |
| 1.    |      |      | Change C45 from SF000002V00 to SF000003X00   |         |
| 2.    |      |      | Change +LCDVDD enable control from EC to LVDS convertor,un-pop R367 and R365 change short pad.   |         |
| 3.    |      |      | <del>Change LCD_BACKLIGHT control from EC to LVDS convertor,un-pop R364 and R363 change 0 ohm.</del>   |         |
| 4.    |      |      | Remove un-used components(U18,R335,R336,C357,C359,C360,R338,R339) for eDP to LVDS convertor.   |         |
| 5.    |      |      | Pop R428 for AZ_SDIN0_HD.  |         |
| 6.    |      |      | U2 footprint change from socket to IC.   |         |
| 7.    |      |      | Add RH11   |         |
| 8.    |      |      | Change Y2 from SJ10000CU00 to SJ10000DE00,change C106 & C107 from 27pF to 4.7pF  |         |
| 9.    |      |      | Change R423 location to L45  |         |
| 10.   |      |      | Change D7 from SC2N202U010 to SC600000B00 for 替代料  |         |
| 11.   |      |      | Change Q29 from SB548000210 to SB000002N00.  |         |
| 12.   |      |      | Change D8&D9 from SCS00002G00 to SCS00000Z00   |         |
| 13.   |      |      | X1 code change:1.Change Q2,Q3,Q4,Q5,Q30,Q31 from SB01000JE00 to SB00000E000. 2.Change Q9 from SB934130020 to SB934130000. 3.Change Q10 from SB00000FC00 to SB00000F400. 4.Change L1 from SM01000JE00 to SB01000JN00. |         |
| 14.   |      |      | Change R551 & R553 pull-high from +3VS to +3VALW_PCH for leakage.  |         |
| 15.   |      |      | Add R677 & R678 & R679 for PTC request, Change R473,R490,R679,R677,R678 from 0ohm to PTC(SP040005X00).   |         |
| 16.   |      |      | Change Q10 from SB00000FC00 to SB00000L800 for 替代料   |         |
| 17.   |      |      | Remove R469 0ohm for TV.   |         |
| 18.   |      |      | Add C2134 ,C2135,C2136,C2137,C2138,C2139,C2140,C2141,C2143 for ESD.  |         |
| 19.   |      |      | Remove JXDP1,OC1,OC2,RC3,RC4,R125,R126.  |         |
| 20.   |      |      | Pop U7&R231, un-pop R228 for PLT_RST_VGA#.   |         |
| 21.   |      |      | Swap SATA_PRX_DTX_N1 & SATA_PRX_DTX_P1 for m-SATA pin define.  |         |
| 22.   |      |      | Un-pop LAN power components Q26,Q27,R573,R574,C562.  |         |
| 23.   |      |      | 0 ohm change to short pad: R347,R585,R507,R674,R644,R645,R646,R647   |         |
| 24.   |      |      | Change R453&R457 from 0ohm to 1.1K, R451&R459 from 300ohm to 5.6Kohm.  |         |
| 25.   |      |      | Pop R438,R439 for ESD request.   |         |

PVT change list:  
1. Change Q10 from SB00000FC00(EOL soon) to SB000002N00(同Q29),SB00000FC00 as 2nd source.Schematic,需驗證

2. Change U23 pin12\_+USB3\_VCCA to +USB3\_VCCB, pop U22, un-pop U24 for USB charger
3. R365 change from short pad to 0ohm.
4. U5 pin5 change from +3VSto +3VALW\_PCH for BCM43142 wake from WLAN issue.
5. Change R473,R490,R677,R678,R679 from SP040005X00\_0603 size to F1,F2,F4,F5,F3 SP040003S00\_1206 size.
6. Change L11 from SM010014520 to SM01000EJ00 for ACL request
7. Change L8 from SM010007W00 to SM010019400 for ACL request
8. Change D7 from SC2N202U010 to SC600000B00(same as D1/D2), SC2N202U010 as 2nd source..
9. Change RP19 from SD309510A80(T88 P/N) to SD309510A10.
11. Change R276 from 10k to 100k for +3VS\_VGA rise time.
12. Change R672 from 10k to 100k for +3VALW\_PCH rise time.
14. Change R438 & R439 from 0\_0603 to short pad.
15. Un-pop C125 & C548 for sequence EA.
16. Change C394, C398,C520 & C514 from 220uF(LELON\_SF000001F00) to 100uF (Panasonic\_SF000005100) to meet Inrush EA & ACL request.
17. Change C170 & C171 from 12pF to 10pF for EA.
20. Change C106 & C107 from 4.7pF to 10pF for 25MHz crystal.
21. Add R677 & reserve R678 on U5 AND gate for PLT\_A\_RST#
13. Change JUSB1 & JUSB2 from DC23300AE00 to DC233008R00(VBA11)
24. Change R591 pull-high from +5VSB to VL for power S5 Erp request.
22. Change D20 & D21 from SC300001Y00 to SC300002F00 for ESD request
23. Change D22 & D23 from SCA00001100 to SCA00000T00 for ESD ACL request
10. Add C2144-C2152 for EMI request.
18. Change R402 from short pad to 22ohm for EMI, R399,R401,R403 & R404 change from short pad to 0 ohm for EMI request.
19. Reserve C2153,C2154,C2155,C2156, add D29 for ESD.
20. Change R282 from 100k to 2k, R277 from 470 to 22 ohm for GPU power sequence.
21. Change Y1 from SJ100001K00 to SJ10000FA00 ,C102 & C107 to 6pF.

- pre-MP change list:
1. Change R399,R401,R402,R403,R404 from 0ohm to short pad.
2. Add C2157 and reserve C2158.
3. Change R8,R470,R669,R670,R416 from 0ohm to short pad.
4. Un-pop JECDB1 & SW1.
5. For R3 P/N, change PCH P/N from SA00006RF00 to SA00006RF20, PCB P/N from DA60011S000 to DA60011S010 and GPU P/N from SA00006ZF00 to SA00006ZF10.
6. Change C520 & C514 from 100uF to 220uF.
7. Pop C2149~C2152 for ESD request.
8. Change C559 & C2128 from 0603 to 0805.
9. Change C2145 from 0.1uF to 470pF, change C2149~C2152 from 330pF to 470pF for EMI.
10. Add C418 for EMI.

|   |                    |                 |            |                          |                             |                |
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|   |                    |                 |            |                          | VCA00 LA-9791P M/B          | 0.3            |
|   |                    |                 |            | Date                     | Tuesday, September 24, 2013 | Sheet 89 of 99 |